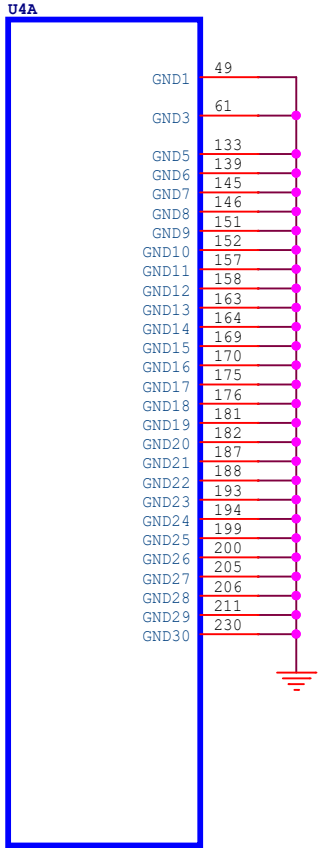


可达鸭  
开源  
祝国  
产芯

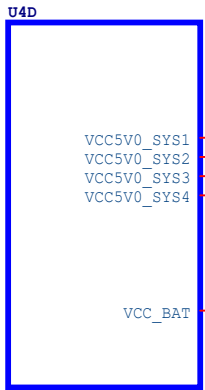
**YYDS**

<b>Hlink H68K-SCH</b>		
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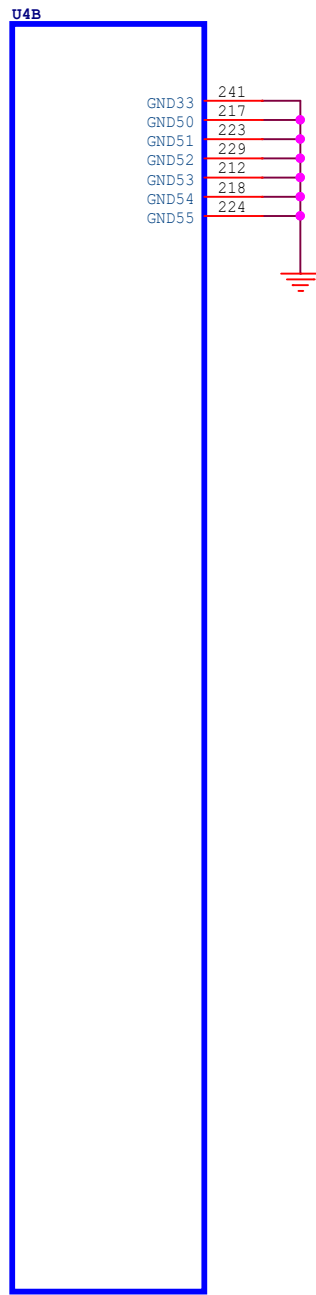
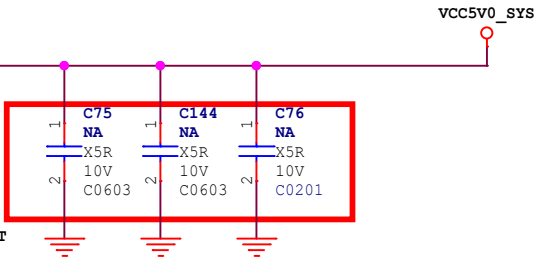
# RK3568\_ABCDE (Power&Gnd)



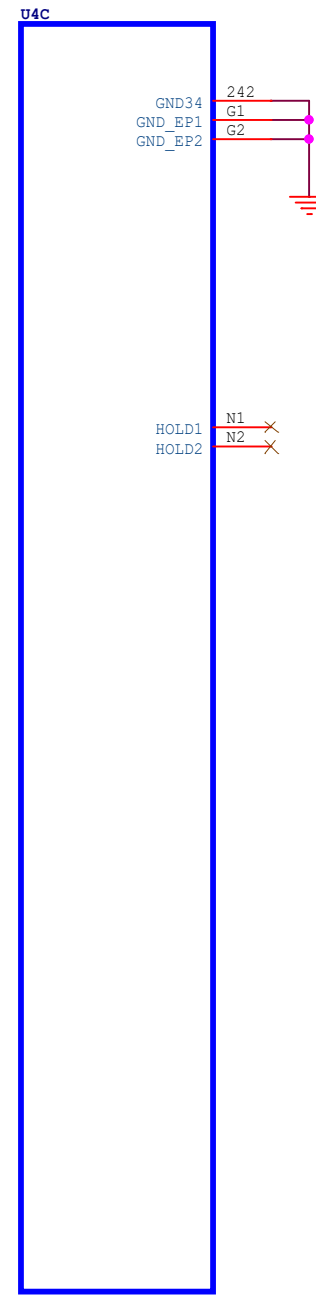
NA  
SCNN\_FOXCONN\_AS0A826



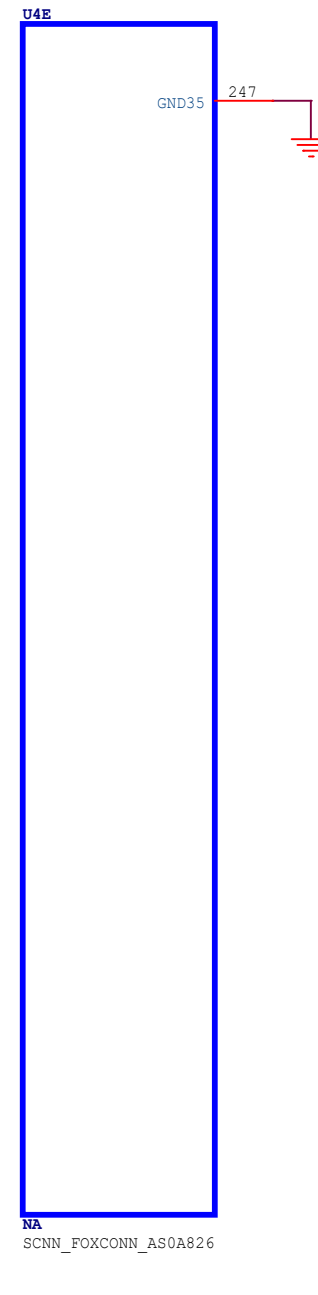
NA  
SCNN\_FOXCONN\_AS0A826



NA  
SCNN\_FOXCONN\_AS0A826



NA  
SCNN\_FOXCONN\_AS0A826



NA  
SCNN\_FOXCONN\_AS0A826

Hlink H68K-SCH

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# RK3568\_F (DDR PHY)

U4F

DDR4	LPDDR4	DDR3	LPDDR3	DDR4	LPDDR4	DDR3	LPDDR3
/ DDR4 DQ10 A	/ LPDDR4 DQ0 A	/ DDR3 DQ0	/ LPDDR3 DQ15	DDR4 A0	/ LPDDR4 CLKP B	/ DDR3 A9	/ --- /
DDR4 DQ12 A	LPDDR4 DQ1 A	DDR3 DQ1	LPDDR3 DQ14	DDR4 A1	---	DDR3 A2	---
DDR4 DQ14 A	LPDDR4 DQ2 A	DDR3 DQ2	LPDDR3 DQ16	DDR4 A2	LPDDR4 A1 A	DDR3 A4	LPDDR3 A6
DDR4 DQ15 A	LPDDR4 DQ3 A	DDR3 DQ3	LPDDR3 DQ17	DDR4 A3	LPDDR4 CKE1 A	DDR3 A3	---
DDR4 DQ16 A	LPDDR4 DQ4 A	DDR3 DQ4	LPDDR3 DQ18	---	---	---	---
DDR4 DQ17 A	LPDDR4 DQ5 A	DDR3 DQ5	LPDDR3 DQ19	DDR4 A4	LPDDR4 A3 B	DDR3 BA1	LPDDR3 A3
DDR4 DQ18 A	LPDDR4 DQ6 A	DDR3 DQ6	LPDDR3 DQ20	DDR4 A5	LPDDR4 A3 B	DDR3 BA1	LPDDR3 A3
DDR4 DQ19 A	LPDDR4 DQ7 A	DDR3 DQ7	LPDDR3 DQ21	DDR4 A6	LPDDR4 A1 B	DDR3 A4	LPDDR3 A6
DDR4 DQ20 A	LPDDR4 DQ8 A	DDR3 DQ8	LPDDR3 DQ22	DDR4 A7	LPDDR4 CKE0 CA B	DDR3 A5	---
---	---	---	---	---	LPDDR4 ODTP CA B	DDR3 A6	---
DDR4 DML A	LPDDR4 DM0 A	DDR3 DM0	LPDDR3 DM1	DDR4 A8	LPDDR4 ODTP CA A	DDR3 A6	LPDDR3 A9
---	---	---	---	DDR4 A9	LPDDR4 CLKN B	DDR3 A5	---
DDR4 DQSL P A	LPDDR4 DQSLP A	DDR3 DQSLP	LPDDR3 DQSLP	DDR4 A10	LPDDR4 CKE0 B	DDR3 A10	---
DDR4 DQSL N A	LPDDR4 DQSLN A	DDR3 DQSLN	LPDDR3 DQSLN	DDR4 A11	LPDDR4 A0 A	DDR3 A7	LPDDR3 A5
---	---	---	---	---	---	---	---
DDR4 DQ03 A	LPDDR4 DQ8 A	DDR3 DQ8	LPDDR3 DQ25	DDR4 A12	LPDDR4 A3 A	DDR3 BA2	---
DDR4 DQ01 A	LPDDR4 DQ9 A	DDR3 DQ9	LPDDR3 DQ24	DDR4 A13	LPDDR4 A0 B	DDR3 A14	LPDDR3 A0
DDR4 DQ07 A	LPDDR4 DQ10 A	DDR3 DQ10	LPDDR3 DQ28	DDR4 A14 WEN	LPDDR4 A4 A	DDR3 A15	LPDDR3 A5
DDR4 DQ05 A	LPDDR4 DQ11 A	DDR3 DQ11	LPDDR3 DQ29	DDR4 A15 CAS	LPDDR4 A2 A	DDR3 A0	---
DDR4 DQ02 A	LPDDR4 DQ12 A	DDR3 DQ12	LPDDR3 DQ28	---	---	---	---
DDR4 DQ04 A	LPDDR4 DQ13 A	DDR3 DQ13	LPDDR3 DQ31	DDR4 A16 RASn	LPDDR4 A5 A	DDR3 RASn	LPDDR3 A7
DDR4 DQ06 A	LPDDR4 DQ14 A	DDR3 DQ14	LPDDR3 DQ30	DDR4 A17	LPDDR4 CKE1 B	DDR3 CASn	---
DDR4 DQ08 A	LPDDR4 DQ15 A	DDR3 DQ15	LPDDR3 DQ27	DDR4 BA0	LPDDR4 A2 B	DDR3 A1	---
---	---	---	---	DDR4 BA1	LPDDR4 A4 B	DDR3 A12	LPDDR3 A4
DDR4 DMU A	LPDDR4 DM1 A	DDR3 DM1	LPDDR3 DM3	DDR4 B0	LPDDR4 ODTP CA B	DDR3 WEN	---
---	---	---	---	DDR4 B1	LPDDR4 ODTP CA A	DDR3 WEN	---
DDR4 DQSU P A	LPDDR4 DQSLP A	DDR3 DQSLP	LPDDR3 DQSLP	DDR4 CKE	LPDDR4 CKE0 A	DDR3 CKE	LPDDR3 CKE
DDR4 DQSU N A	LPDDR4 DQSLN A	DDR3 DQSLN	LPDDR3 DQSLN	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 DQ07 B	LPDDR4 DQ0 B	DDR3 DQ16	LPDDR3 DQ1	DDR4 CLKP	LPDDR4 CLKP A	DDR3 CLKP	LPDDR3 CLKP
DDR4 DQ05 B	LPDDR4 DQ1 B	DDR3 DQ17	LPDDR3 DQ2	DDR4 CLKN	LPDDR4 CLKN A	DDR3 CLKN	LPDDR3 CLKN
DDR4 DQ03 B	LPDDR4 DQ2 B	DDR3 DQ18	LPDDR3 DQ3	---	---	---	---
DDR4 DQ01 B	LPDDR4 DQ3 B	DDR3 DQ19	LPDDR3 DQ4	DDR4 CS0n	LPDDR4 CS0n A	DDR3 ODTP	LPDDR3 ODTP
DDR4 DQ04 B	LPDDR4 DQ4 B	DDR3 DQ20	LPDDR3 DQ7	DDR4 CS1n	LPDDR4 CS1n A	DDR3 CS1n	LPDDR3 CS1n
DDR4 DQ06 B	LPDDR4 DQ5 B	DDR3 DQ21	LPDDR3 DQ8	DDR4 ODTP	LPDDR4 CS1n B	DDR3 ODTP	LPDDR3 CS1n
DDR4 DQ08 B	LPDDR4 DQ6 B	DDR3 DQ22	LPDDR3 DQ9	DDR4 CS2n	LPDDR4 CS2n B	DDR3 CS2n	LPDDR3 CS2n
DDR4 DQ02 B	LPDDR4 DQ7 B	DDR3 DQ23	LPDDR3 DQ0	---	---	---	---
---	---	---	---	DDR4 RESETn	LPDDR4 RESETn	DDR3 RESETn	---
DDR4 DMU B	LPDDR4 DM0 B	DDR3 DM2	LPDDR3 DM0	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 DQSU P B	LPDDR4 DQSLP B	DDR3 DQSLP	LPDDR3 DQSLP	---	---	---	---
DDR4 DQSU N B	LPDDR4 DQSLN B	DDR3 DQSLN	LPDDR3 DQSLN	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 DQ10 B	LPDDR4 DQ8 B	DDR3 DQ24	LPDDR3 DQ18	---	---	---	---
DDR4 DQ12 B	LPDDR4 DQ9 B	DDR3 DQ25	LPDDR3 DQ19	---	---	---	---
DDR4 DQ14 B	LPDDR4 DQ10 B	DDR3 DQ26	LPDDR3 DQ22	---	---	---	---
DDR4 DQ16 B	LPDDR4 DQ11 B	DDR3 DQ27	LPDDR3 DQ23	---	---	---	---
DDR4 DQ17 B	LPDDR4 DQ12 B	DDR3 DQ28	LPDDR3 DQ18	---	---	---	---
DDR4 DQ15 B	LPDDR4 DQ13 B	DDR3 DQ29	LPDDR3 DQ17	---	---	---	---
DDR4 DQ11 B	LPDDR4 DQ14 B	DDR3 DQ30	LPDDR3 DQ20	---	---	---	---
DDR4 DQ13 B	LPDDR4 DQ15 B	DDR3 DQ31	LPDDR3 DQ21	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 DML B	LPDDR4 DM1 B	DDR3 DM3	LPDDR3 DM2	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 DQSL P B	LPDDR4 DQSLP B	DDR3 DQSLP	LPDDR3 DQSLP	---	---	---	---
DDR4 DQSL N B	LPDDR4 DQSLN B	DDR3 DQSLN	LPDDR3 DQSLN	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 ECC DQ7	/ --	/ DDR3 ECC DQ0	---	---	---	---	---
DDR4 ECC DQ0	/ --	/ DDR3 ECC DQ1	---	---	---	---	---
DDR4 ECC E02	/ --	/ DDR3 ECC DQ2	---	---	---	---	---
DDR4 ECC DQ1	/ --	/ DDR3 ECC DQ3	---	---	---	---	---
DDR4 ECC DQ6	/ --	/ DDR3 ECC DQ4	---	---	---	---	---
DDR4 ECC DQ4	/ --	/ DDR3 ECC DQ5	---	---	---	---	---
DDR4 ECC DQ3	/ --	/ DDR3 ECC DQ6	---	---	---	---	---
DDR4 ECC DQ2	/ --	/ DDR3 ECC DQ7	---	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 ECC DM	/ --	/ DDR3 ECC DM	---	---	---	---	---
---	---	---	---	---	---	---	---
DDR4 ECC DQ5 P	/ --	/ DDR3 ECC DQ5 P	---	---	---	---	---
DDR4 ECC DQ5 N	/ --	/ DDR3 ECC DQ5 N	---	---	---	---	---

NA  
SCNN\_FOXCNN\_AS0A826

Note: Sequences can not be swap

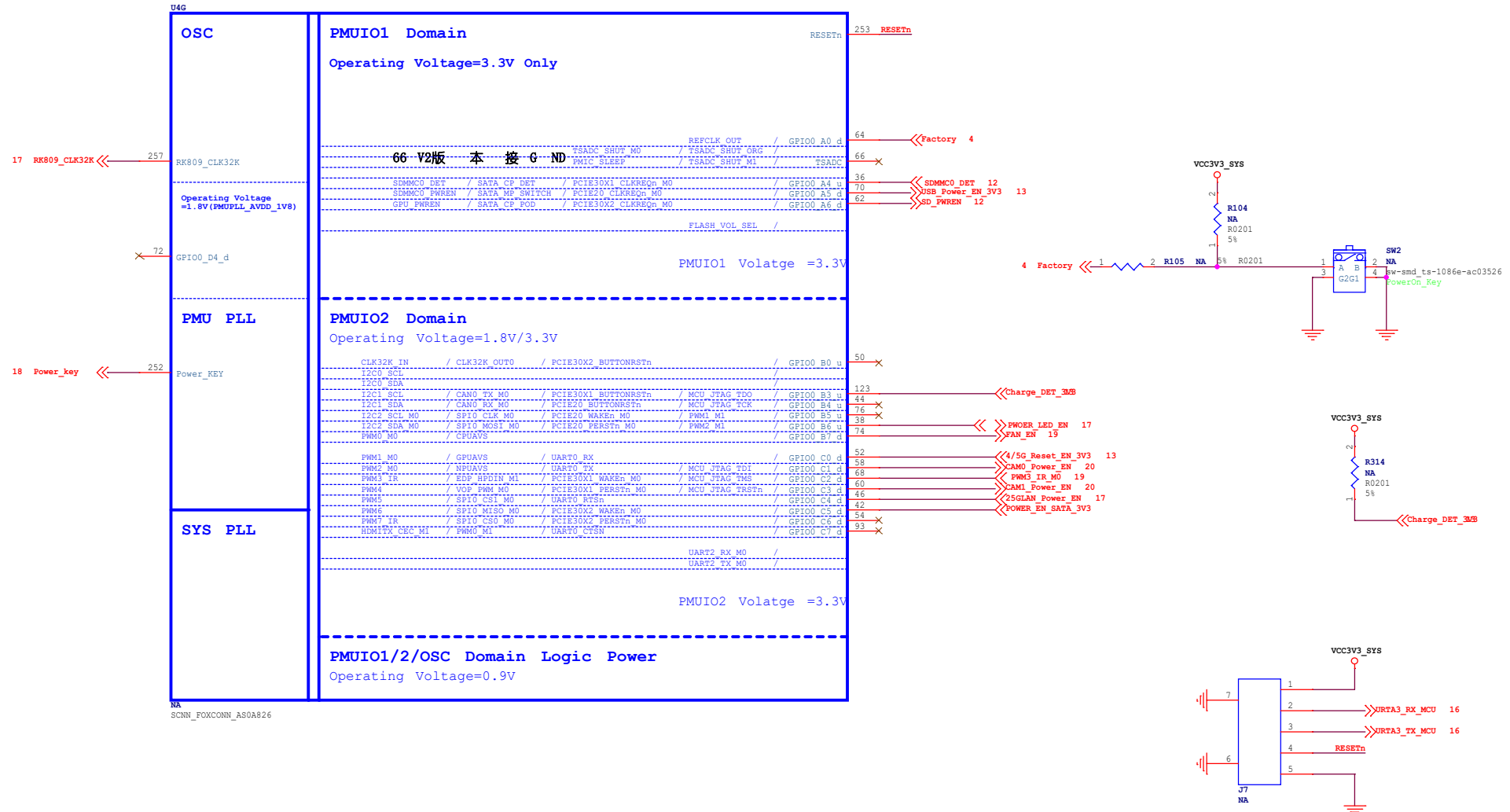


DDR3L =1.35V  
DDR3 =1.5V  
DDR4 =1.2V  
LPDDR3 =1.2V  
LPDDR4 =1.1V  
LPDDR4x =1.1V

DDR3L =1.35V  
DDR3 =1.5V  
DDR4 =1.2V  
LPDDR3 =1.2V  
LPDDR4 =1.1V  
LPDDR4x =0.6V

Note:  
Except DDR3, other DQ sequences  
can not be swap

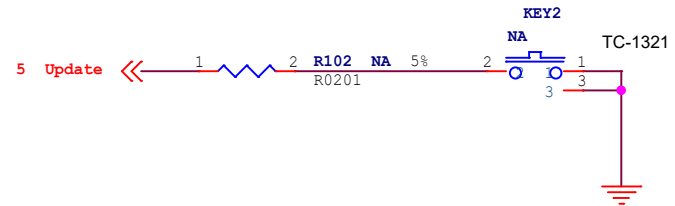
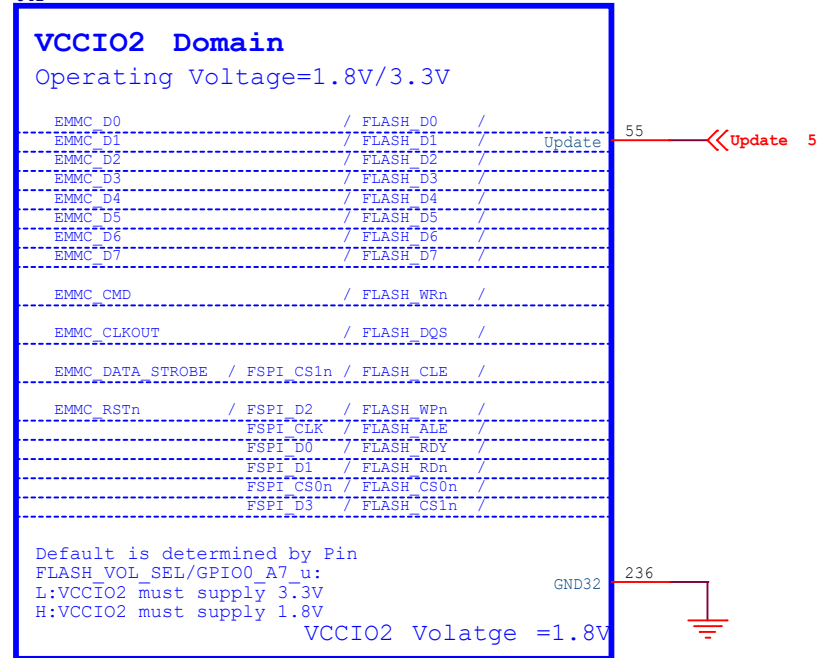
# RK3568\_G (OSC/PLL/PMUIO1/2)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

# RK3568\_I (VCCIO2 Domain)

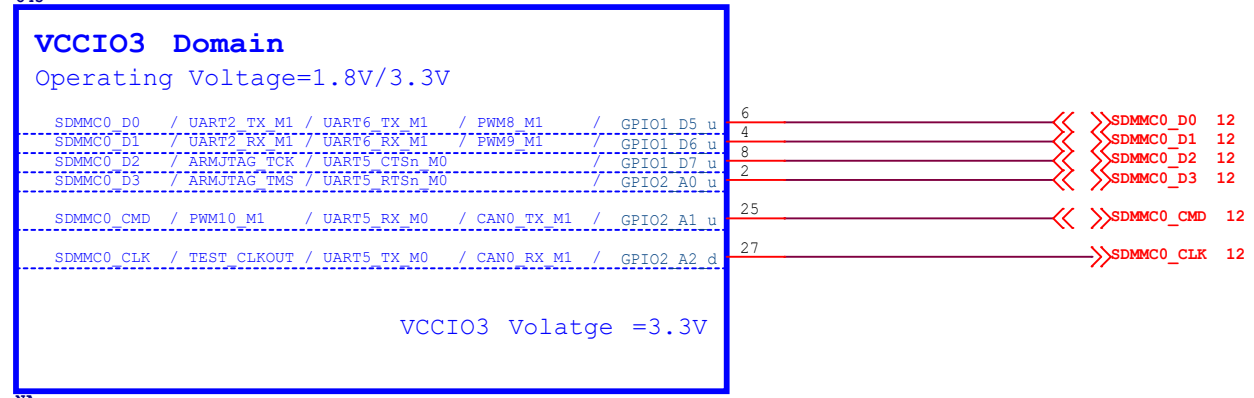
U4I



NA  
SCNN\_FOXCONN\_AS0A826

# RK3568\_J (VCCIO3 Domain)

U4J

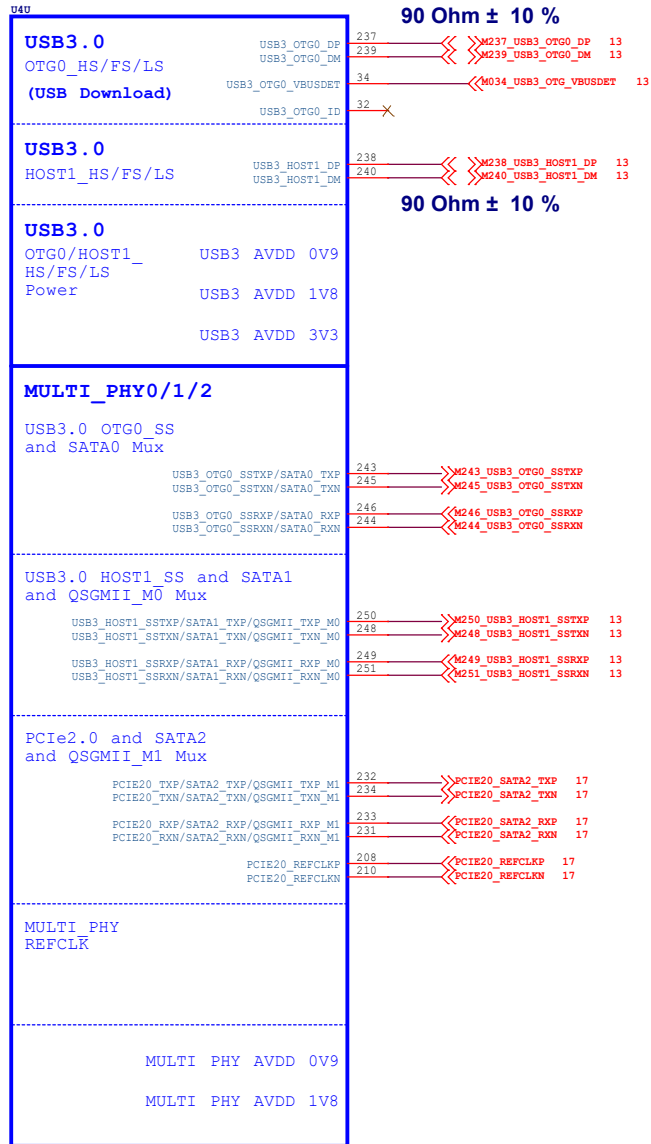


NA  
SCNN\_FOXCONN\_AS0A826

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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# RK3568\_U (USB3.0/SATA/QSGMII/PCIE2.0 x1)



TO SATA

TO USB3.0-A 5G LTE

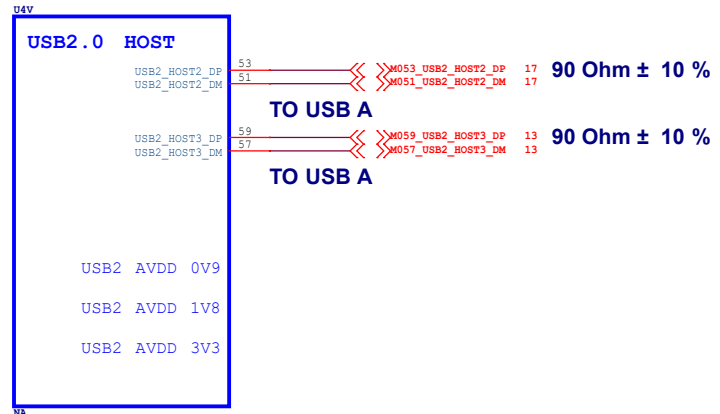
TO M2 WIFI

NA  
SCNN\_FOXCNN\_A50A826

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

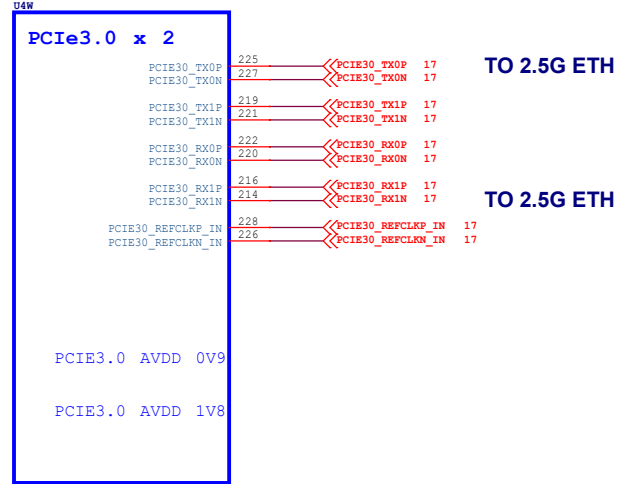
**Rockchip Confidential**

# RK3568\_V (USB2.0 HOST)



NA  
SCNN\_FOXCNN\_A50A826

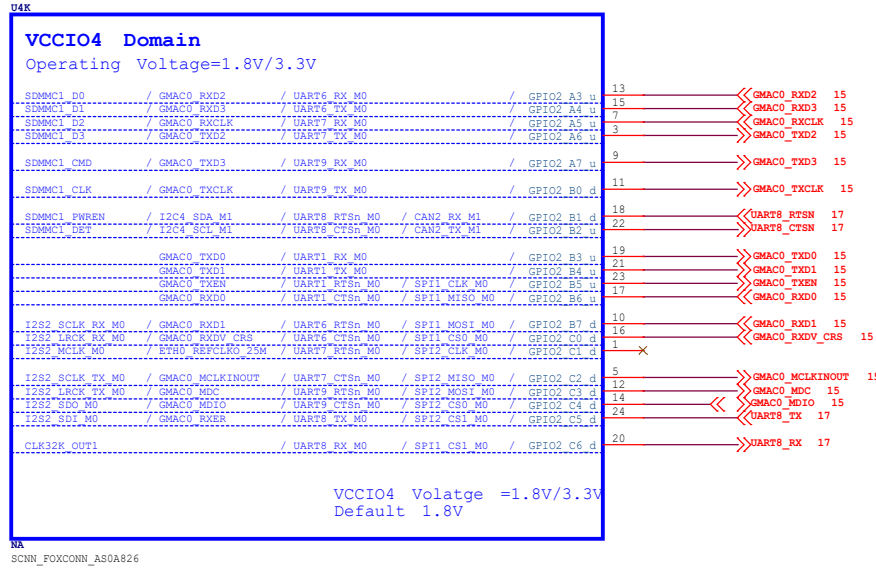
# RK3568\_W (PCIE3.0 x2)



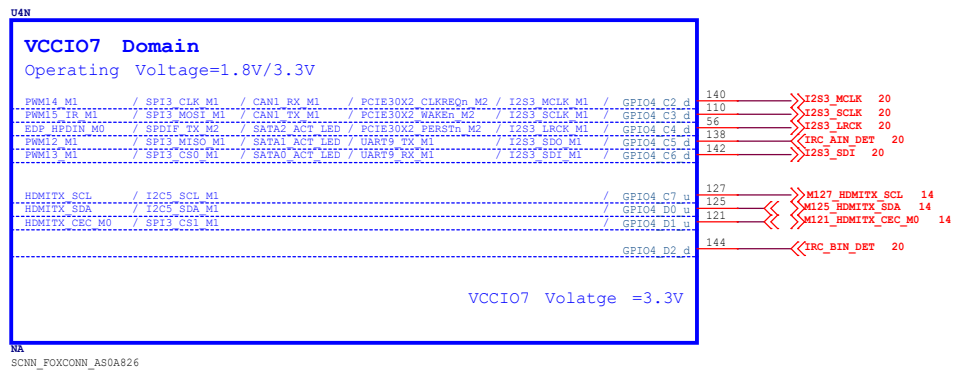
NA  
SCNN\_FOXCNN\_A50A826

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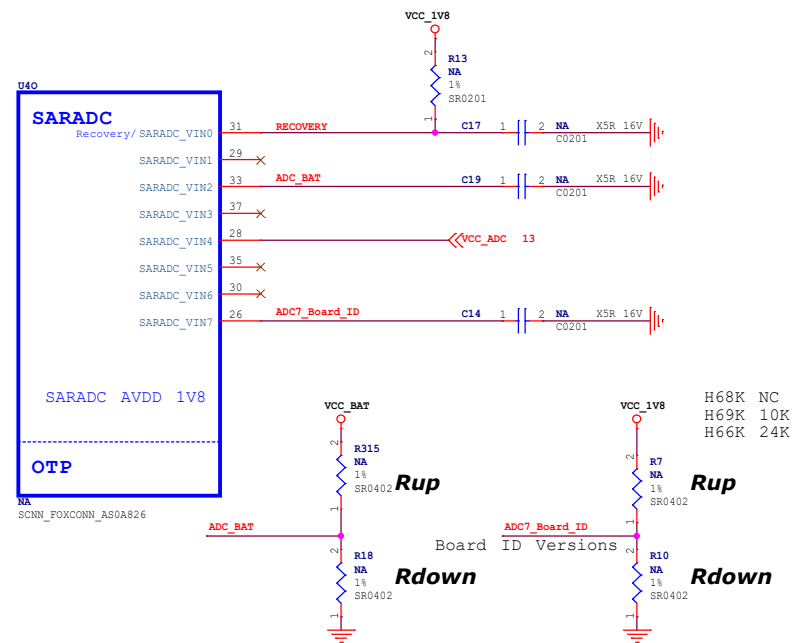
# RK3568\_K (VCCIO4 Domain)



# RK3568\_N (VCCIO7 Domain)



# RK3568\_O (SARADC/OTP)



# RK3568\_P (MIPI\_CSI\_RX)

U4P

## MIPI CSI RX

MIPI_CSI_RX_D0P	147	>>>MIPI_CSI_RX0_D0P	20
MIPI_CSI_RX_D0N	149	>>>MIPI_CSI_RX0_D0N	20
MIPI_CSI_RX_D1P	141	>>>MIPI_CSI_RX0_D1P	20
MIPI_CSI_RX_D1N	143	>>>MIPI_CSI_RX0_D1N	20
MIPI_CSI_RX_D2P	154	>>>MIPI_CSI_RX0_D2P	20
MIPI_CSI_RX_D2N	156	>>>MIPI_CSI_RX0_D2N	20
MIPI_CSI_RX_D3P	150	>>>MIPI_CSI_RX0_D3P	20
MIPI_CSI_RX_D3N	148	>>>MIPI_CSI_RX0_D3N	20
MIPI_CSI_RX_CLK0P	135	>>>MIPI_CSI_RX0_CLKP	20
MIPI_CSI_RX_CLK0N	137	>>>MIPI_CSI_RX0_CLKN	20
MIPI_CSI_RX_CLK1P	129	>>>MIPI_CSI_RX1_CLKP	20
MIPI_CSI_RX_CLK1N	131	>>>MIPI_CSI_RX1_CLKN	20

## MIPI CSI

MIPI CSI RX AVDD 0V9

MIPI CSI RX AVDD 1V8

NA  
SCNN\_FOXCNN\_A50A826

# RK3568\_M (VCCIO6 Domain)

U4M

## VCCIO6 Domain

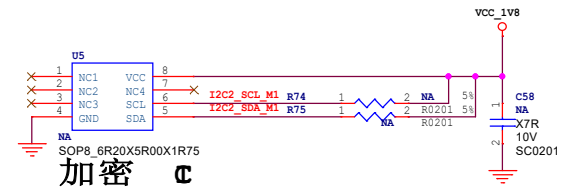
Operating Voltage=1.8V/3.3V

CIF_D0	/ EBC_SDD00 / SDMMC2_D0_M0	/ I2S1_MCLK_M1	/ VOP_BT656_D0_M1	/ GPIO3_C6_d	118	>>>SDIO_D0	17
CIF_D1	/ EBC_SDD01 / SDMMC2_D1_M0	/ I2S1_SCLK_TX_M1	/ VOP_BT656_D1_M1	/ GPIO3_C7_d	106	>>>SDIO_D1	17
CIF_D2	/ EBC_SDD02 / SDMMC2_D2_M0	/ I2S1_LRCK_TX_M1	/ VOP_BT656_D2_M1	/ GPIO3_D0_d	83	>>>SDIO_D2	17
CIF_D3	/ EBC_SDD03 / SDMMC2_D3_M0	/ I2S1_SDO0_M1	/ VOP_BT656_D3_M1	/ GPIO3_D1_d	81	>>>SDIO_D3	17
CIF_D4	/ EBC_SDD04 / SDMMC2_CMD_M0	/ I2S1_SDI0_M1	/ VOP_BT656_D4_M1	/ GPIO3_D2_d	92	>>>SDIO_CMD	17
CIF_D5	/ EBC_SDD05 / SDMMC2_CLK_M0	/ I2S1_SDI1_M1	/ VOP_BT656_D5_M1	/ GPIO3_D3_d	85	>>>SDIO_CLK	17
CIF_D6	/ EBC_SDD06 / SDMMC2_DEP_M0	/ I2S1_SDI2_M1	/ VOP_BT656_D6_M1	/ GPIO3_D4_d	77	>>>WIFI_WAKE_HOST	17
CIF_D7	/ EBC_SDD07 / SDMMC2_PWREN_M0	/ I2S1_SDI3_M1	/ VOP_BT656_D7_M1	/ GPIO3_D5_d	104	>>>HOST_WAKE_WIFI	17
CIF_D8	/ EBC_SDD08 / GMAC1_TXD2_M1	/ UART1_TX_M1	/ PFM_CLK0_M1	/ GPIO3_D6_d	94	>>>GMAC1_TXD2	16
CIF_D9	/ EBC_SDD09 / GMAC1_TXD3_M1	/ UART1_RX_M1	/ PFM_SDI0_M1	/ GPIO3_D7_d	100	>>>GMAC1_TXD3	16
CIF_D10	/ EBC_SDD10 / GMAC1_RXD1P_M1	/ UART1_TX_M2	/ PFM_CLK1_M1	/ GPIO4_A0_d	102	>>>GMAC1_TXCLK	16
CIF_D11	/ EBC_SDD11 / GMAC1_RXD2_M1	/ UART1_RX_M2	/ PFM_SDI1_M1	/ GPIO4_A1_d	79	>>>GMAC1_RXD2	16
CIF_D12	/ EBC_SDD12 / GMAC1_RXD3_M1	/ UART1_TX_M2	/ PFM_SDI2_M1	/ GPIO4_A2_d	96	>>>GMAC1_RXD3	16
CIF_D13	/ EBC_SDD13 / GMAC1_RXCLK_M1	/ UART1_RX_M2	/ PFM_SDI3_M1	/ GPIO4_A3_d	98	>>>GMAC1_RXCLK	16
CIF_D14	/ EBC_SDD14 / GMAC1_TXD1_M1	/ UART1_TX_M2	/ I2S2_LRCK_TX_M1	/ GPIO4_A4_d	75	>>>GMAC1_TXD0	16
CIF_D15	/ EBC_SDD15 / GMAC1_TXD1_M1	/ UART1_RX_M2	/ I2S2_LRCK_RX_M1	/ GPIO4_A5_d	73	>>>GMAC1_TXD1	16
ISP_FLASHTRIGOUT	/ EBC_SDCE0 / GMAC1_TXEN_M1	/ SPI3_CS0_M0	/ I2S1_SCLK_RX_M1	/ GPIO4_A6_d	71	>>>GMAC1_TXEN	16
CAM_CLKROUT0	/ EBC_SDCE1 / GMAC1_RXD0_M1	/ SPI3_CS1_M0	/ I2S1_LRCK_RX_M1	/ GPIO4_A7_d	69	>>>GMAC1_RXD0	16
CAM_CLKROUT1	/ EBC_SDCE2 / GMAC1_RXD1_M1	/ SPI3_CS2_M0	/ I2S1_SDI0_M1	/ GPIO4_B0_d	78	>>>GMAC1_RXD1	16
ISP_PRELIGHT_TRIG	/ EBC_SDCE3 / GMAC1_RXDV_CRS_M1	/ SPI3_CS0_M1	/ I2S1_SDO2_M1	/ GPIO4_B1_d	67	>>>GMAC1_RXDV_CRS	16
I2C4_SDA_M0	/ EBC_VCOM / GMAC1_RXER_M1	/ SPI3_MOSI_M0	/ I2S2_SDI_M1	/ GPIO4_B2_d	90	>>>MIPICAM0_RST_L	20
I2C4_SCL_M0	/ EBC_GDDE / ETH1_REFCLK0_25M_M1	/ SPI3_CLK_M0	/ I2S2_SDO_M1	/ GPIO4_B3_d	65	>>>MIPICAM1_RST_L	20
I2C2_SDA_M1	/ EBC_GDSE / CAN2_RX_M0	/ ISP_FLASH_TRIGIN	/ VOP_BT656_CLK_M1	/ GPIO4_B4_d	86	>>>I2C2_SDA_M1	20
I2C2_SCL_M1	/ EBC_SDSH / CAN2_TX_M0	/ CAN2_TX_M0	/ I2S1_SDI0_M1	/ GPIO4_B5_d	88	>>>I2C2_SCL_M1	20
CIF_HREF	/ EBC_SDLE / GMAC1_MDC_M1	/ UART1_RTSn_M1	/ I2S2_MCLK_M1	/ GPIO4_B6_d	80	>>>GMAC1_MDC	16
CIF_VSYN	/ EBC_SDCE / GMAC1_MDIO_M1	/ UART1_CTSn_M1	/ I2S2_SCLK_TX_M1	/ GPIO4_B7_d	82	>>>GMAC1_MDIO	16
CIF_CLKOUT	/ EBC_GDCLK	/ PWM11_IR_M1	/	/ GPIO4_C0_d	84	>>>	
CIF_CLKIN	/ EBC_SDCLK / GMAC1_MCLKINOUT_M1	/ UART1_CTSn_M1	/ I2S2_SCLK_RX_M1	/ GPIO4_C1_d	63	>>>GMAC1_MCLKINOUT	16

VCCIO6 Volatge =1.8V/3.3V  
Default 1.8V

## MIPI CSI

NA  
SCNN\_FOXCNN\_A50A826



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# RK3568\_R (MIPI\_DSI\_TX0/LVDS\_TX0)

U4R

## MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	177
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	179
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P	171
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	173
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	159
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	161
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	153
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	155
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP	165
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	167

MIPI DSI TX0/LVDS TX0 AVDD 0V9

MIPI DSI TX0/LVDS TX0 AVDD 1V8

NA  
SCNN\_FOXCCONN\_A50A826

# RK3568\_S (MIPI\_DSI\_TX1)

U4S

## MIPI DSI TX1

MIPI_DSI_TX1_D0P	184
MIPI_DSI_TX1_D0N	186
MIPI_DSI_TX1_D1P	180
MIPI_DSI_TX1_D1N	178
MIPI_DSI_TX1_D2P	168
MIPI_DSI_TX1_D2N	166
MIPI_DSI_TX1_D3P	160
MIPI_DSI_TX1_D3N	162
MIPI_DSI_TX1_CLKP	174
MIPI_DSI_TX1_CLKN	172

MIPI DSI TX1 AVDD 0V9

MIPI DSI TX1 AVDD 1V8

NA  
SCNN\_FOXCCONN\_A50A826

# RK3568\_T (eDP TX)

U4T

## eDP\_TX

eDP_TX_D0P	196
eDP_TX_D0N	198
eDP_TX_D1P	202
eDP_TX_D1N	204
eDP_TX_D2P	207
eDP_TX_D2N	209
eDP_TX_D3P	213
eDP_TX_D3N	215
eDP_TX_AUXP	190
eDP_TX_AUXN	192

eDP TX AVDD 0V9

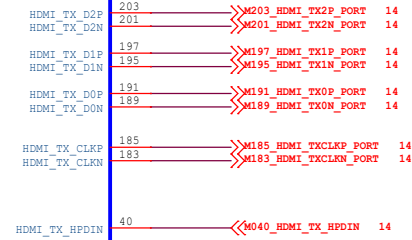
eDP TX AVDD 1V8

NA  
SCNN\_FOXCCONN\_A50A826

# RK3568\_Q (HDMI2.0 TX)

U4Q

## HDMI2.0 TX



MIPI CSI RX AVDD 0V9

MIPI CSI RX AVDD 1V8

NA  
SCNN\_FOXCCONN\_A50A826

HDMI TMDS trace  
100 Ohm ± 10 %

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

# RK3568\_H (VCCIO1 Domain)

U4H

## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/	UART3_RX_M0	/	CAN1_RX_M0	/	AUDIOPWM_LOUT_P	/	ACODEC_ADC_DATA	/	GPI01_A0_u	43
I2C3_SCL_M0	/	UART3_TX_M0	/	CAN1_TX_M0	/	AUDIOPWM_LOUT_N	/	ACODEC_ADC_CLK	/	GPI01_A1_u	47
I2S1_MCLK_M0	/	UART3_RTSn_M0	/	SCR_CLK	/	PCIE30X1_PERSTn_M2	/		/		
I2S1_SCLK_TX_M0	/	UART3_CTSn_M0	/	SCR_IO	/	PCIE30X1_WAKEn_M2	/	ACODEC_DAC_CLK	/		39
I2S1_SCLK_RX_M0	/	UART4_RX_M0	/	PDM_CLK1_M0	/	SPDIF_TX_M0	/		/	GPI01_A4_d	
I2S1_LRCK_TX_M0	/	UART4_RTSn_M0	/	SCR_RST	/	PCIE30X1_CLKREQn_M2	/	ACODEC_DAC_SYNC	/		
I2S1_LRCK_RX_M0	/	UART4_TX_M0	/	PDM_CLK0_M0	/	AUDIOPWM_ROUT_P	/		/		
I2S1_SDO0_M0	/	UART4_CTSn_M0	/	SCR_DET	/	AUDIOPWM_ROUT_N	/	ACODEC_DAC_DATA1	/		41
I2S1_SDI0_M0	/	I2S1_SDI3_M0	/	PDM_SDI3_M0	/	PCIE20_CLKREQn_M2	/	ACODEC_DAC_DATA0	/	GPI01_B0_d	45
I2S1_SDO2_M0	/	I2S1_SDI2_M0	/	PDM_SDI2_M0	/	PCIE20_WAKEn_M2	/	ACODEC_ADC_SYNC	/	GPI01_B1_d	255
I2S1_SDO3_M0	/	I2S1_SDI1_M0	/	PDM_SDI1_M0	/	PCIE20_PERSTn_M2	/		/	GPI01_B2_d	
		I2S1_SDI0_M0	/	PDM_SDI0_M0	/		/		/		

>>>URTA3\_RX\_MCU 16  
>>>URTA3\_TX\_MCU 16

>>>GMAC1\_RSTn 16

VCCIO1 Volatge =1.8V/3.3V  
Default 3.3V

NA

SCNN\_FOXCONN\_AS0A826

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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# RK3568\_L (VCCIO5 Domain)

U4L

## VCCIO5 Domain

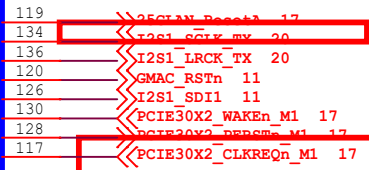
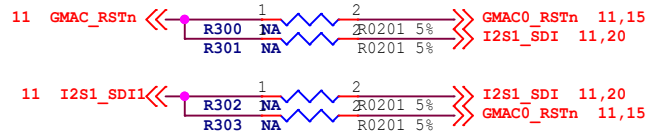
Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLK0_25M_M0	/ SDMMC2_PWREN_M1	/ GPIO3_B0_d	
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPBDF_TX_M1	/ GMAC1_MBI0_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5 Volatge =1.8V/3.3V  
Default 1.8V

金手指要 改为 3V 3

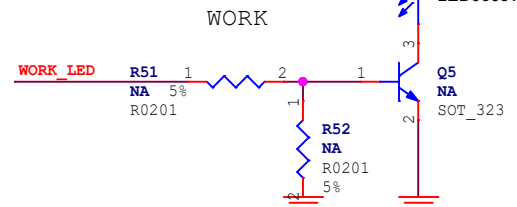
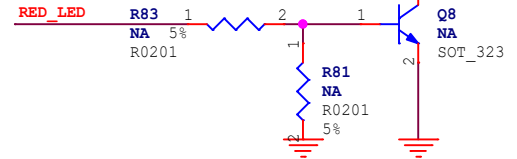
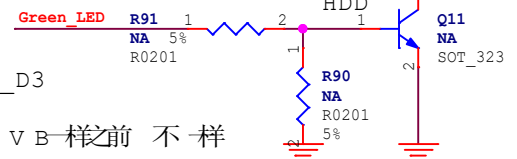
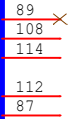
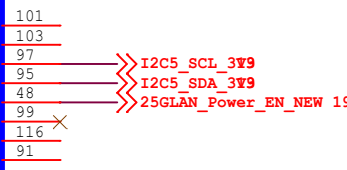
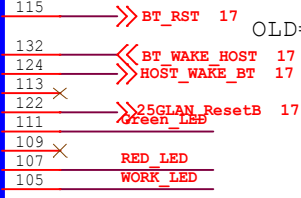
NA  
SCNN\_FOXCONN\_AS0A826



OLD=GPIO2\_D3

B T 与 E V B 样前 不一样

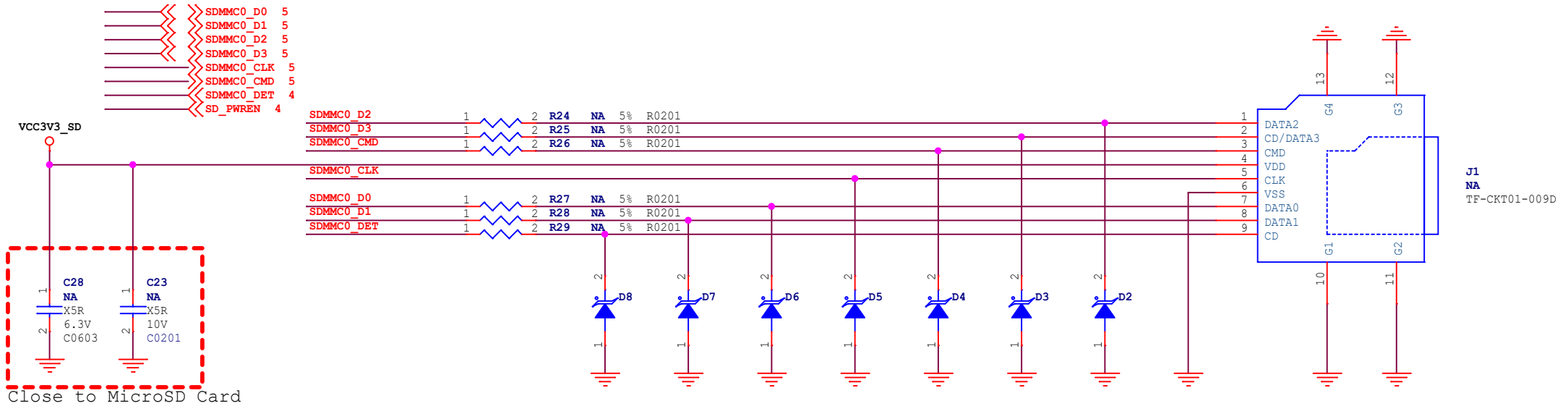
OLD=GPIO2\_D4



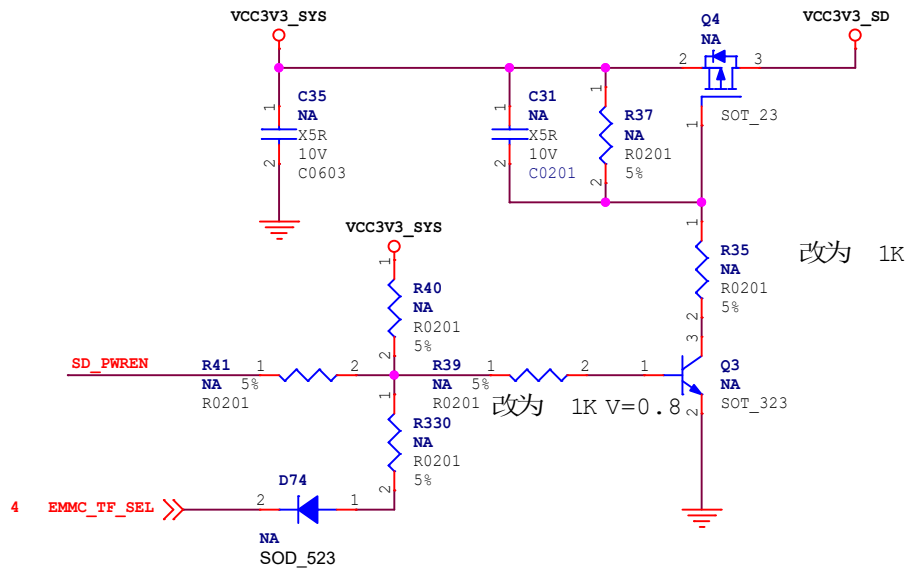
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

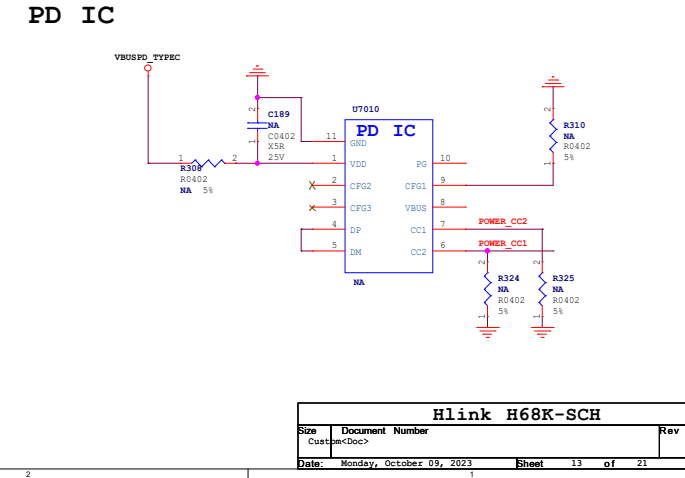
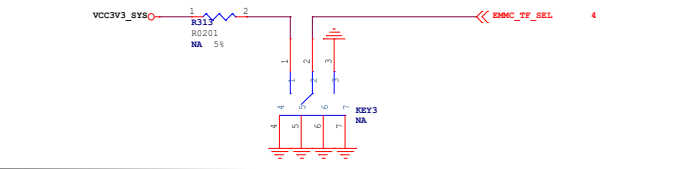
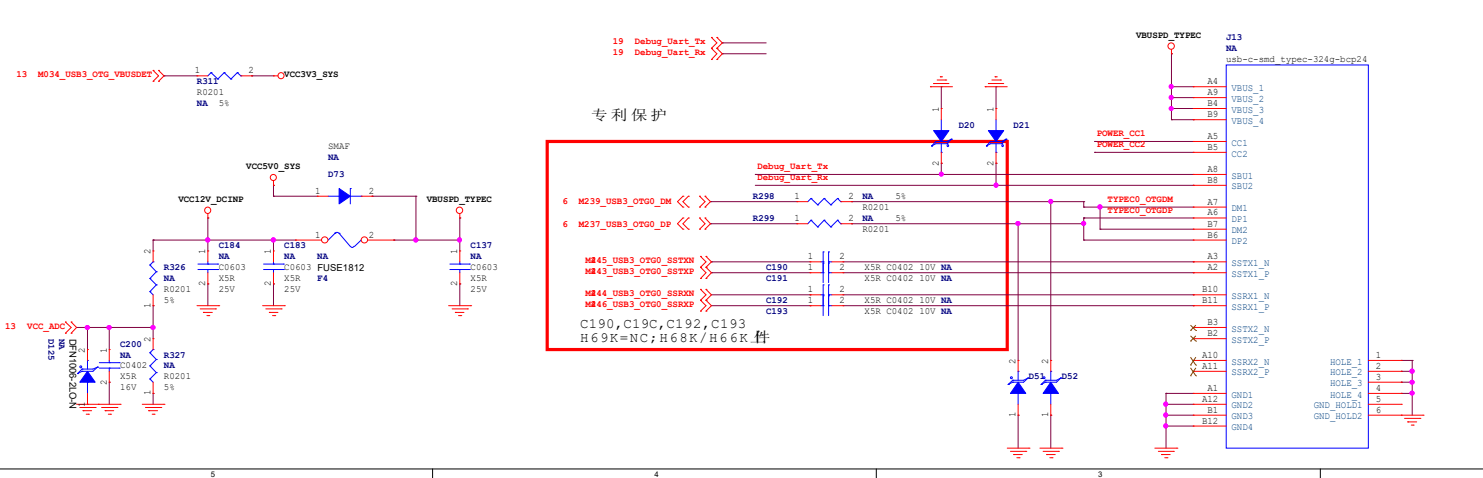
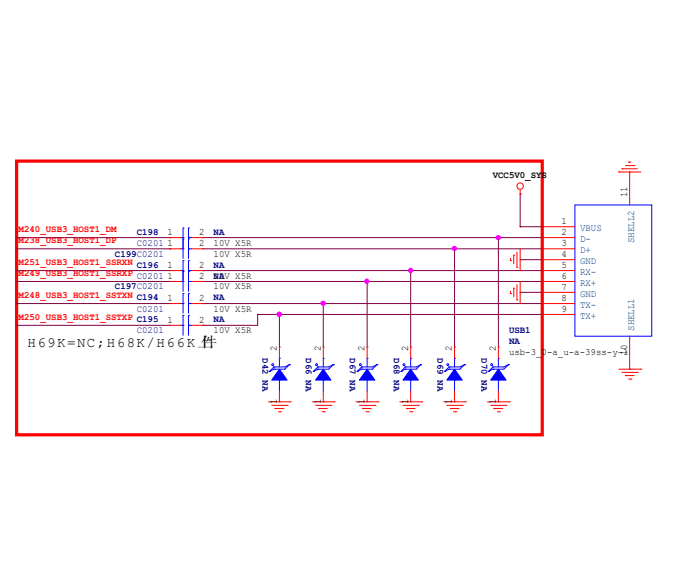
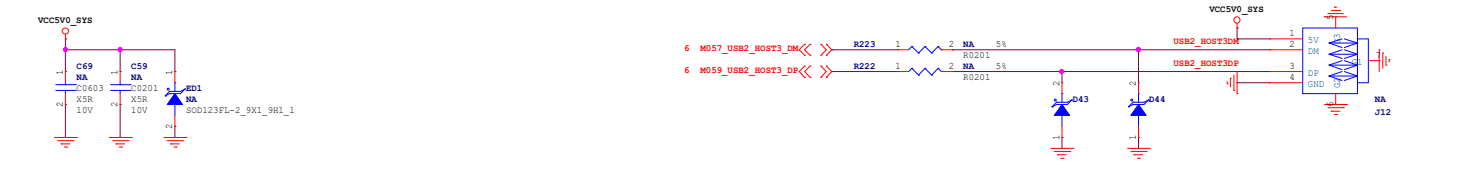
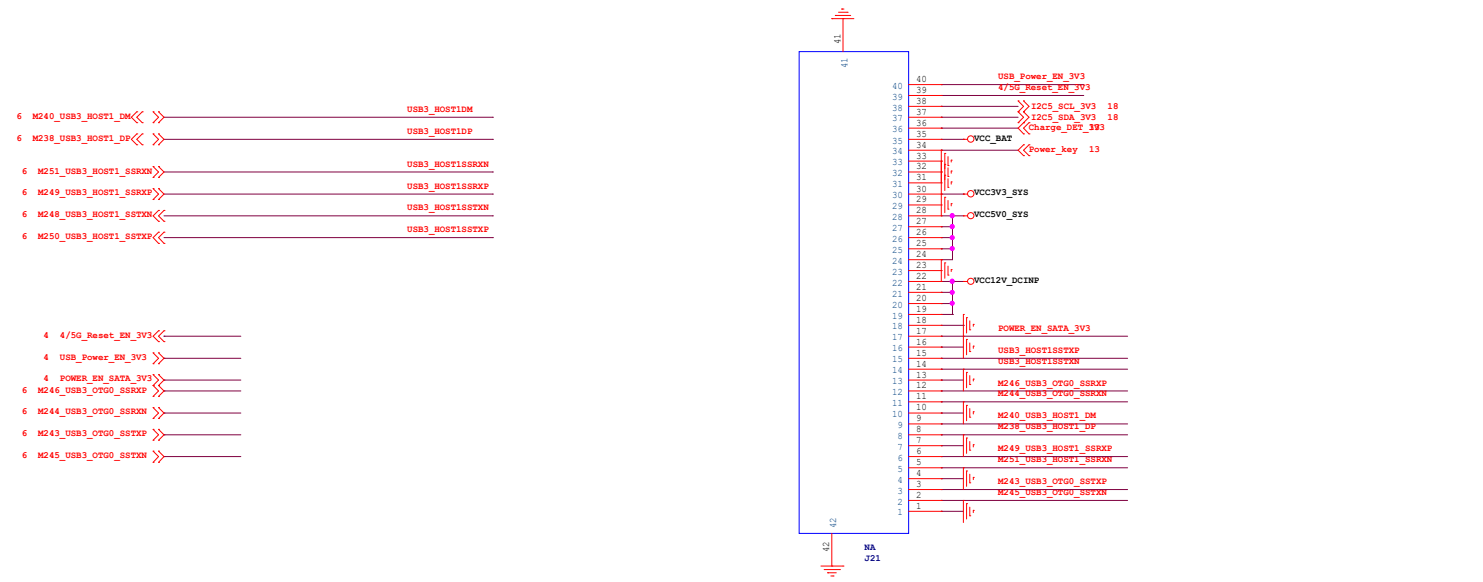
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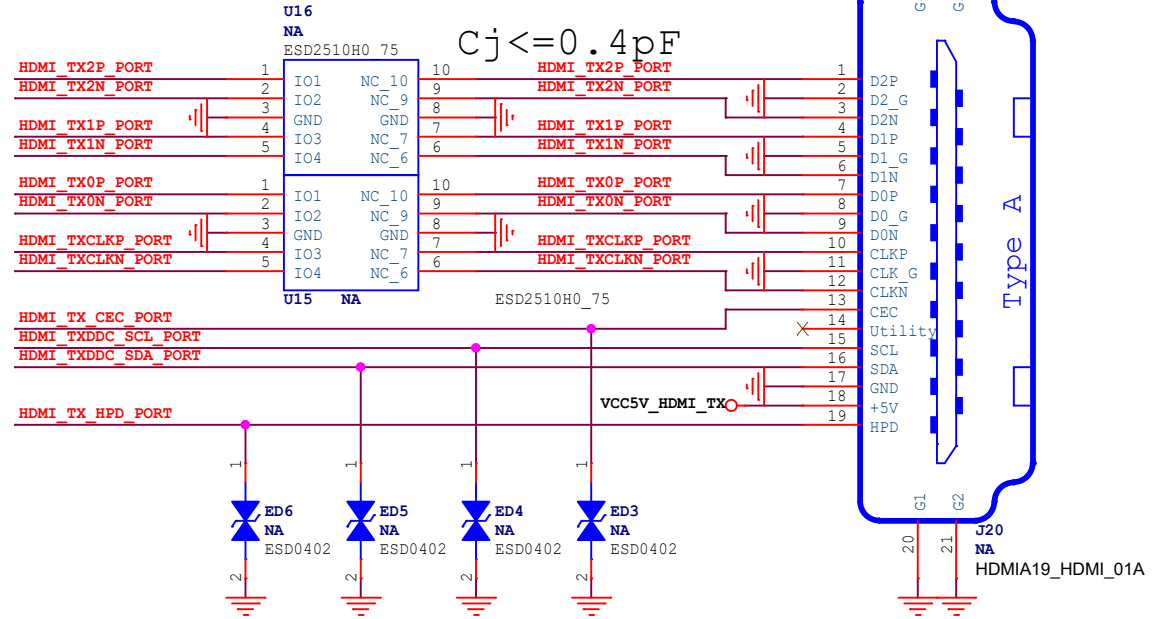
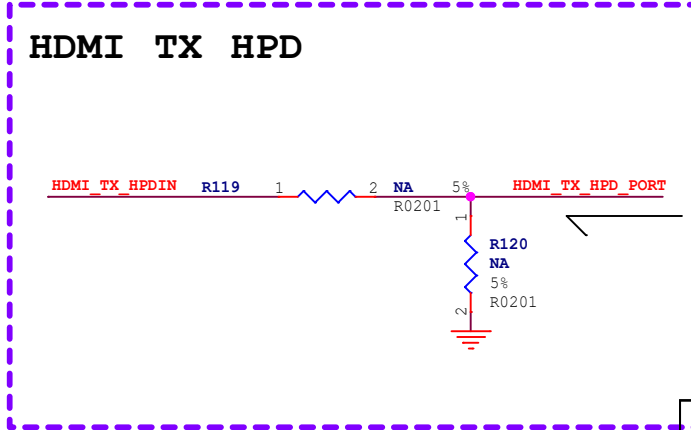
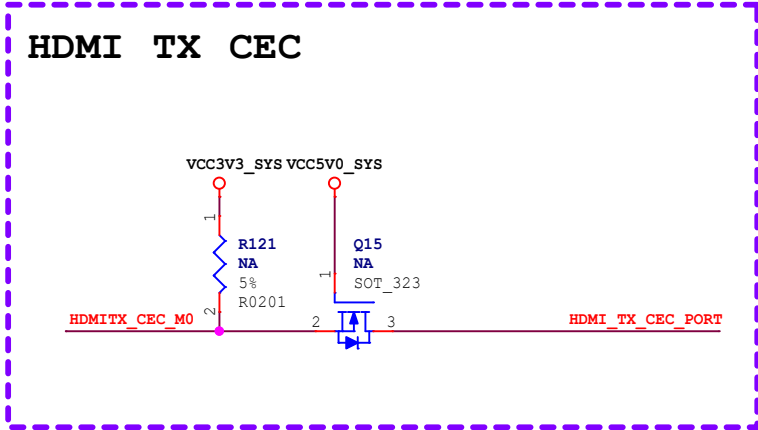
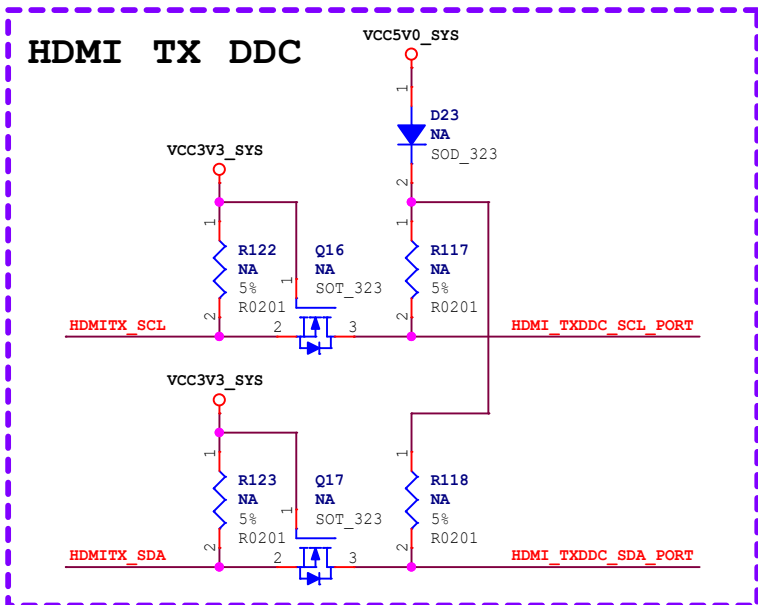
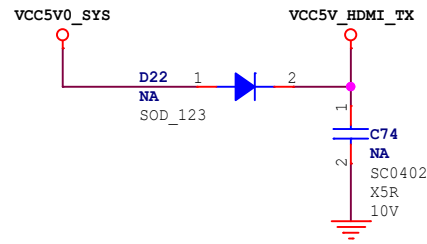
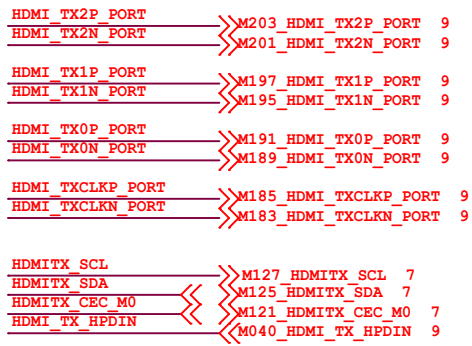


MicroSD Card



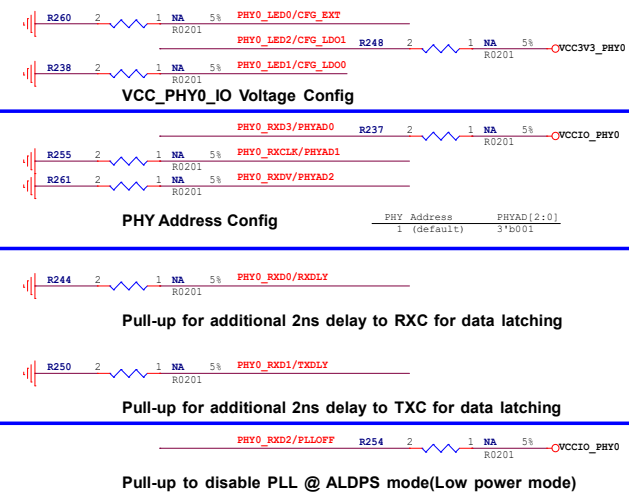
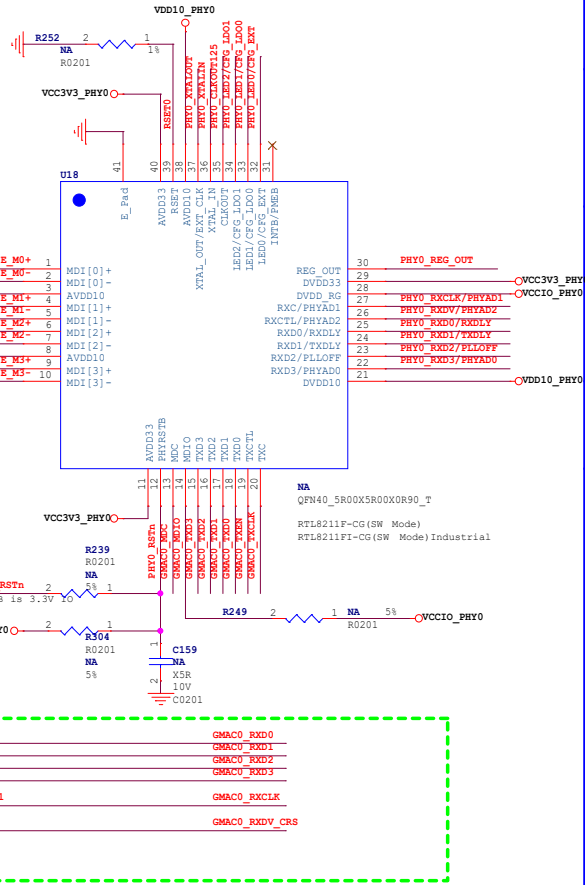
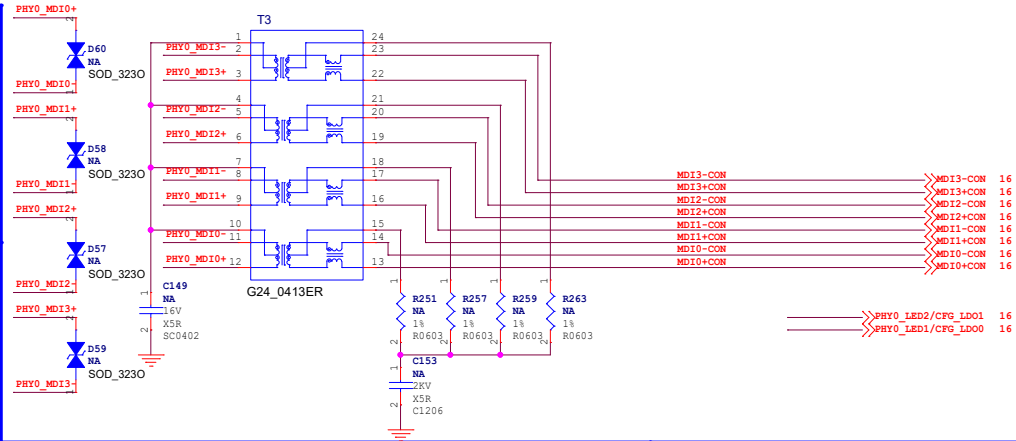
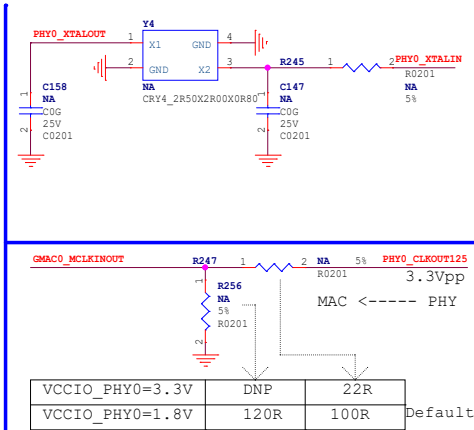
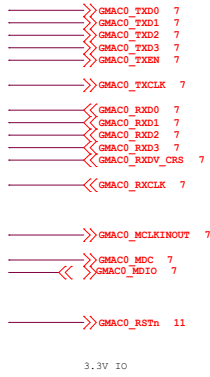


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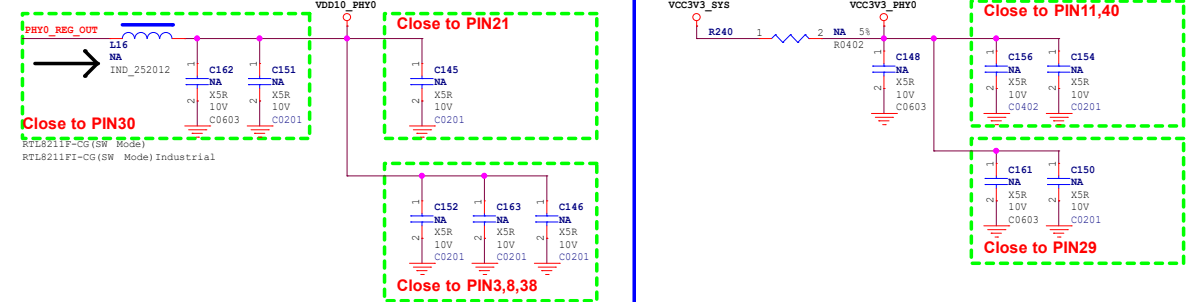


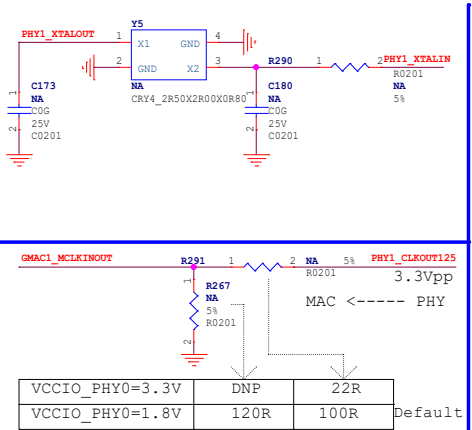
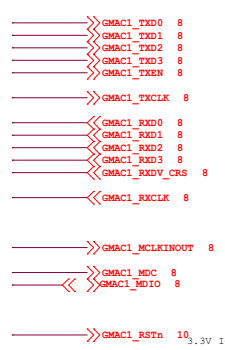
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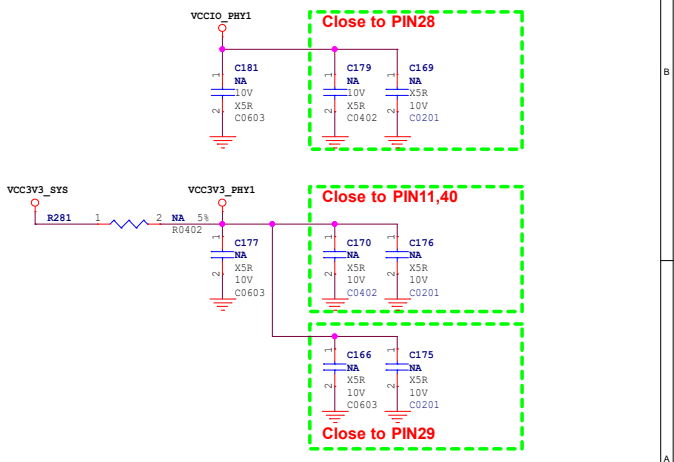
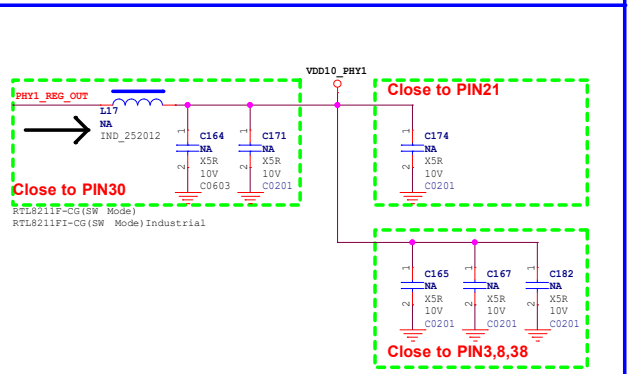
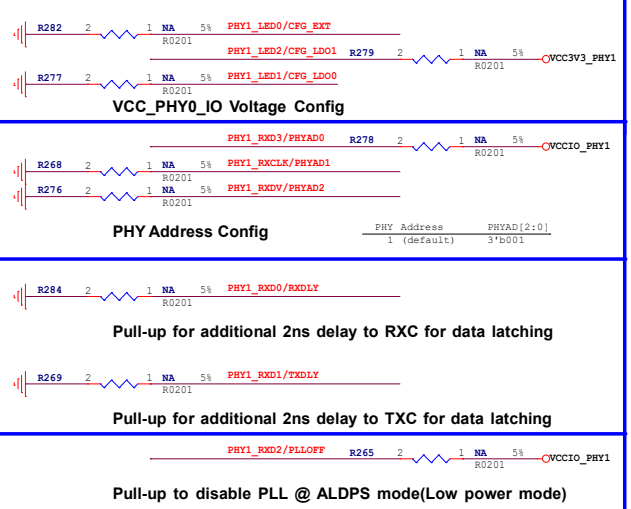
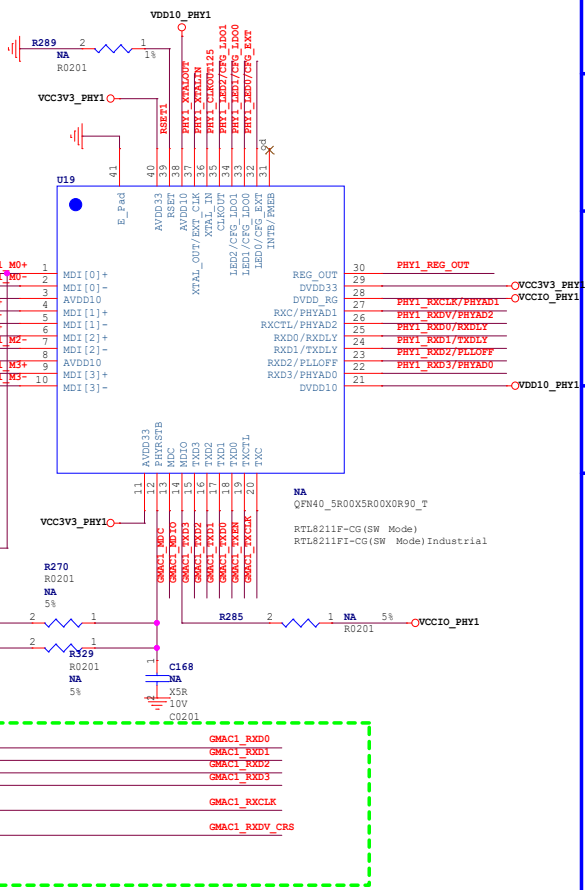
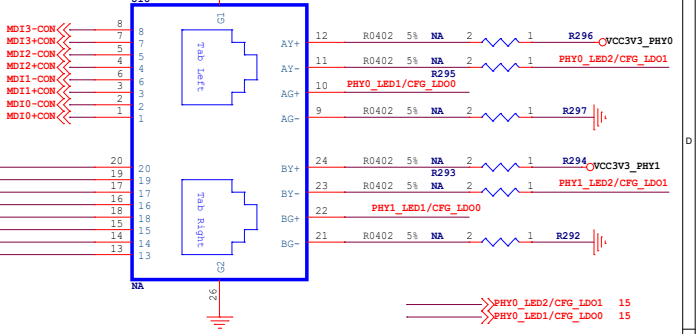
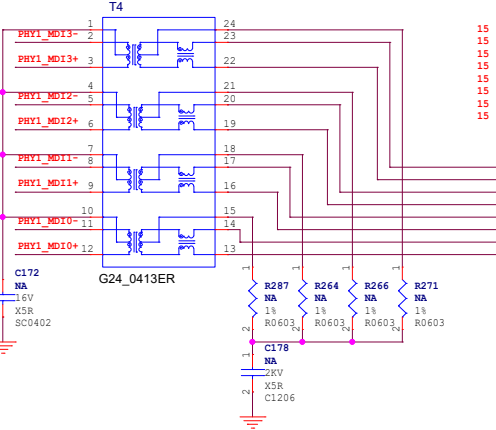
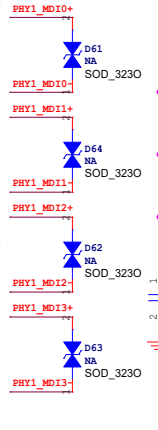


RGMI1 Power Source	CFG EXT	CFG LDO[110]
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 1.8V	1'b0	2'b10





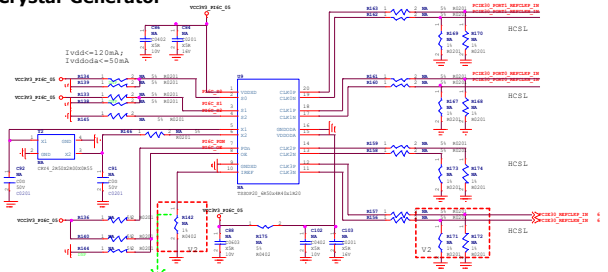
VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default



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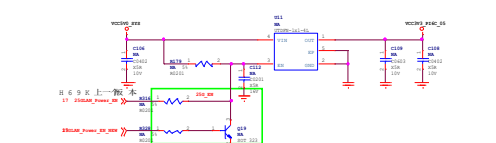
# Crystal Generator



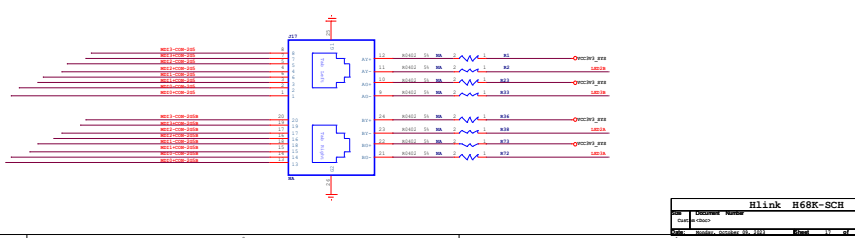
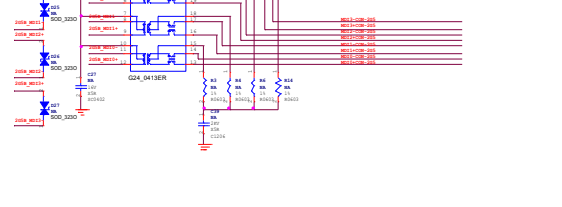
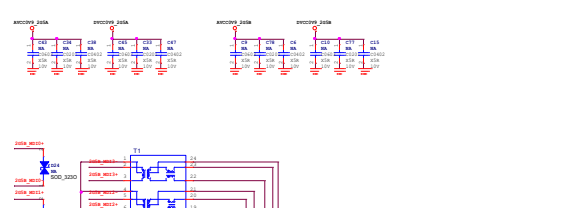
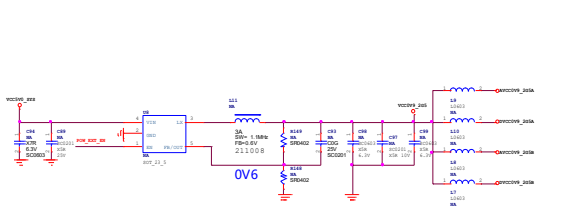
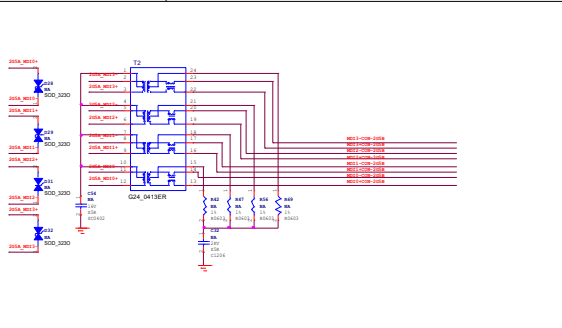
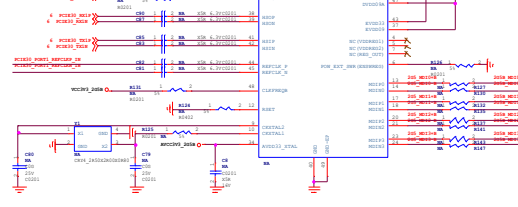
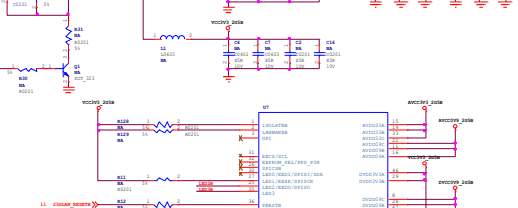
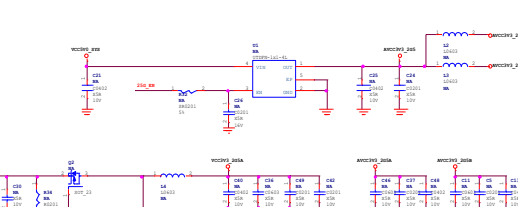
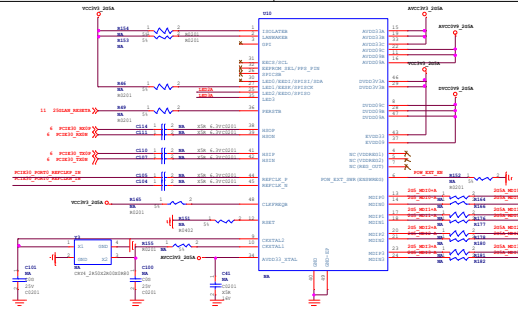
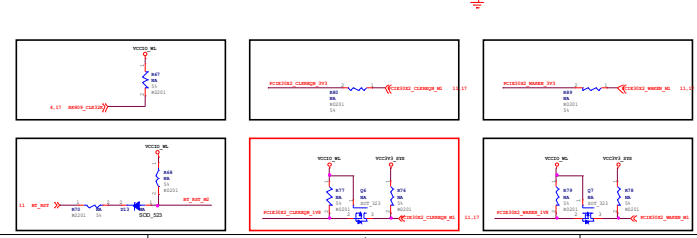
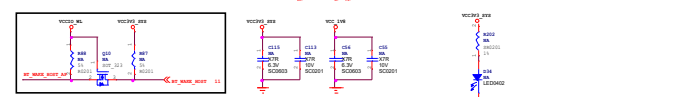
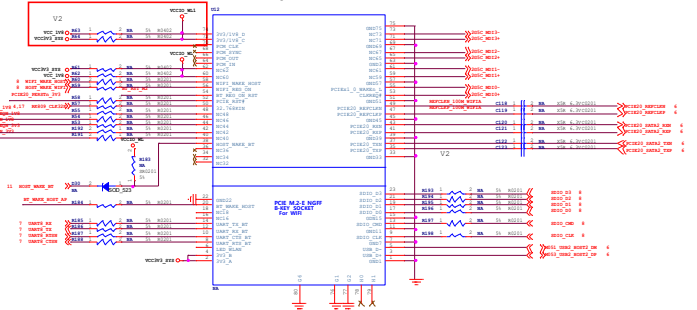
Spread Selection Table:

SS0	SS1	Spread (%)
0	0	Carrier +/- 0.25
0	1	0.5%
1	0	0.5%
1	1	No Spread

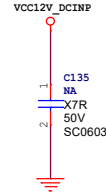
If board target trace impedance is 50ohm then S = 4750ohm providing an IREF of 2.32 mA. The output capacitance (COUT) is 6 \* IREF / Vin=6\*2.32\*50=696pF



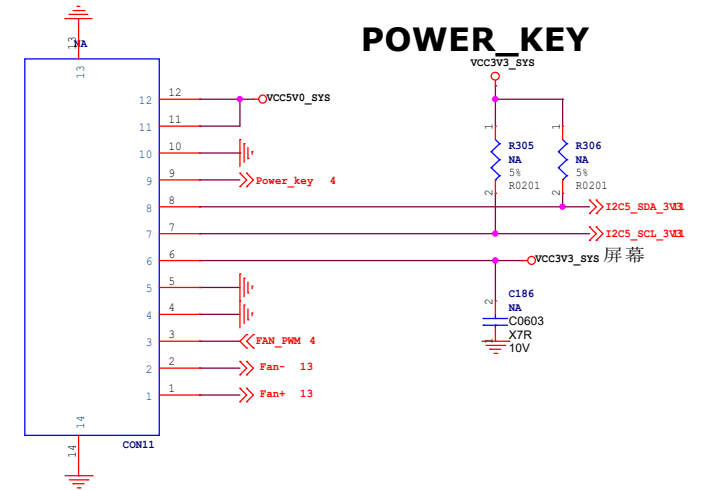
# PCIe WIFI6/BT Module-2T2R



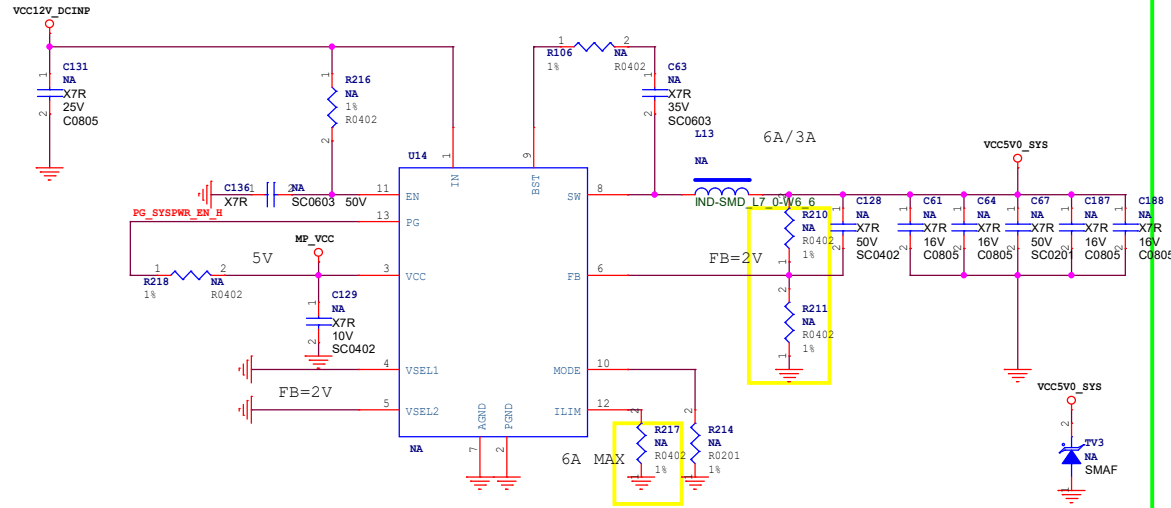
# 12-24V/1A DCIN



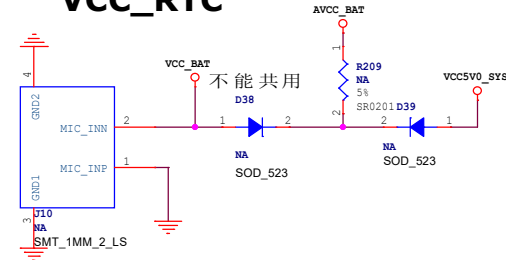
# POWER\_KEY



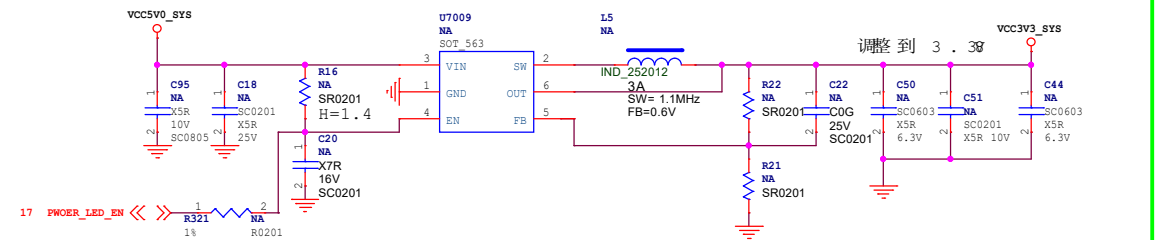
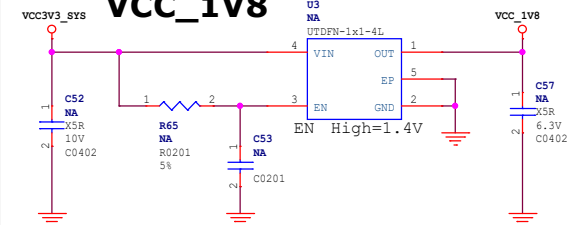
# VCC5V0\_SYS



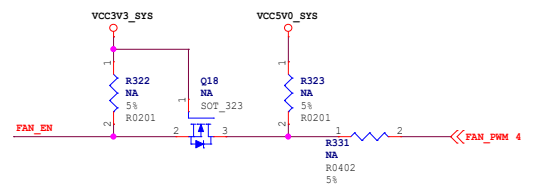
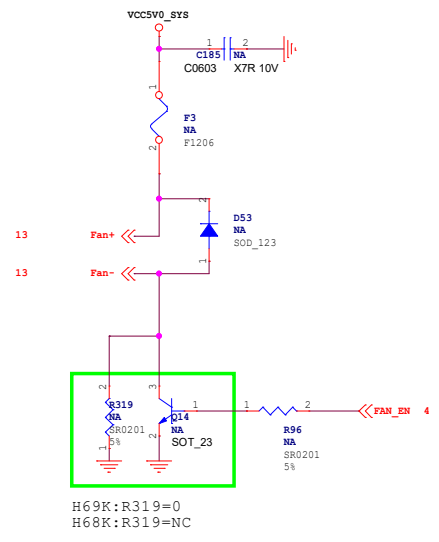
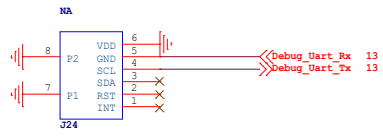
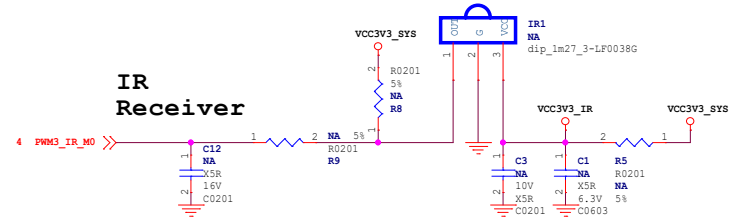
# VCC\_RTC



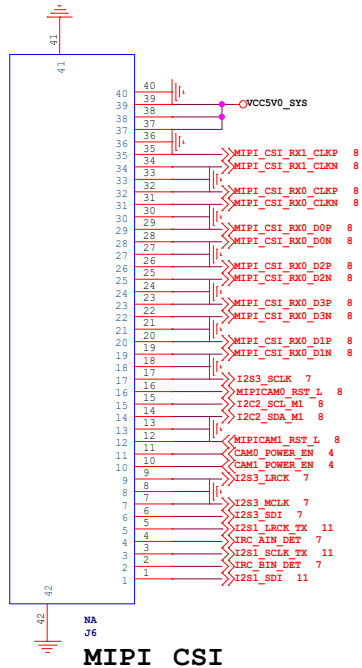
# VCC\_1V8



Hlink H68K-SCH



H69K:R319=0  
H68K:R319=NC



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