Reference Schematics For RK3528

RK3528_BOX_REF_SCH_V10

Main Functions Introduction

1) Power: DiscretePower:BUCK+LDO or PMIC RK805-6
2) RAM: DDR3 4x16bit
   DDR4 2x16Bit
   DDR4 4x16Bit
   LPDDR3 1x32bit
   LPDDR4/LPDDR4X 1x32bit
3) ROM: eMMC5.1 or FSPI Flash
4) Support: Micro SD Card3.0
5) Support: 1 x USB3.0 OTG + 1 x USB2.0 HOST
6) Support: 1 x HDMI2.0 TX
7) Support: 1 x AV OUT
8) Support: SDIO WiFi5 + UART/PCM BT
   PCIE WIFI5 + UART/PCM BT
9) Support: 1 x Ethernet(Embed PHY) + 1x Ethernet(RGMII or RMII)
10) Support: Optical S/PDIF TX
11) Support: IR Receiver
12) Support: Audio-MicArray 2xI2S-DMIC or 4xPDM-DMIC
13) Support: RECOVER/RESET/SARADC_BOOT_KEY,HW_ID
14) Support: 1 x PCIE2.0 Slot
15) Support: Debug UART

HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	00.Cover Page		
Date:	Thursday, February 06, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	1 of 27

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

HINLINK		
Project:	RK3528_H29K	HINLINK
File:	01.Index and Notes	
Date:	Thursday, February 06, 2025	Rev: <Revision>
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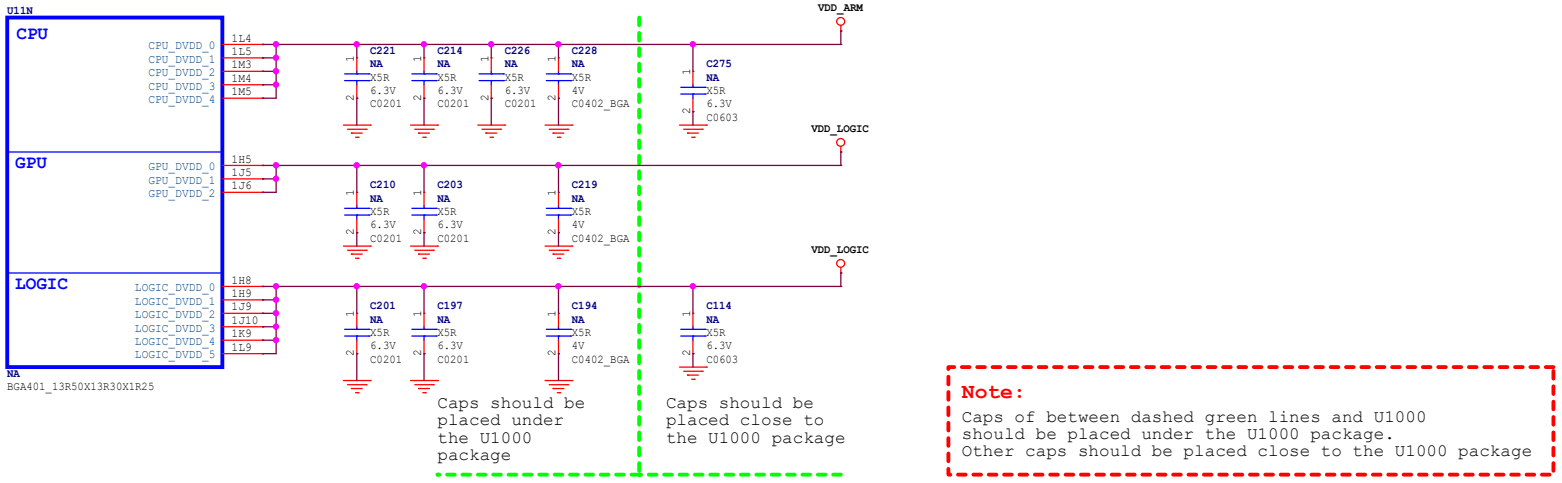
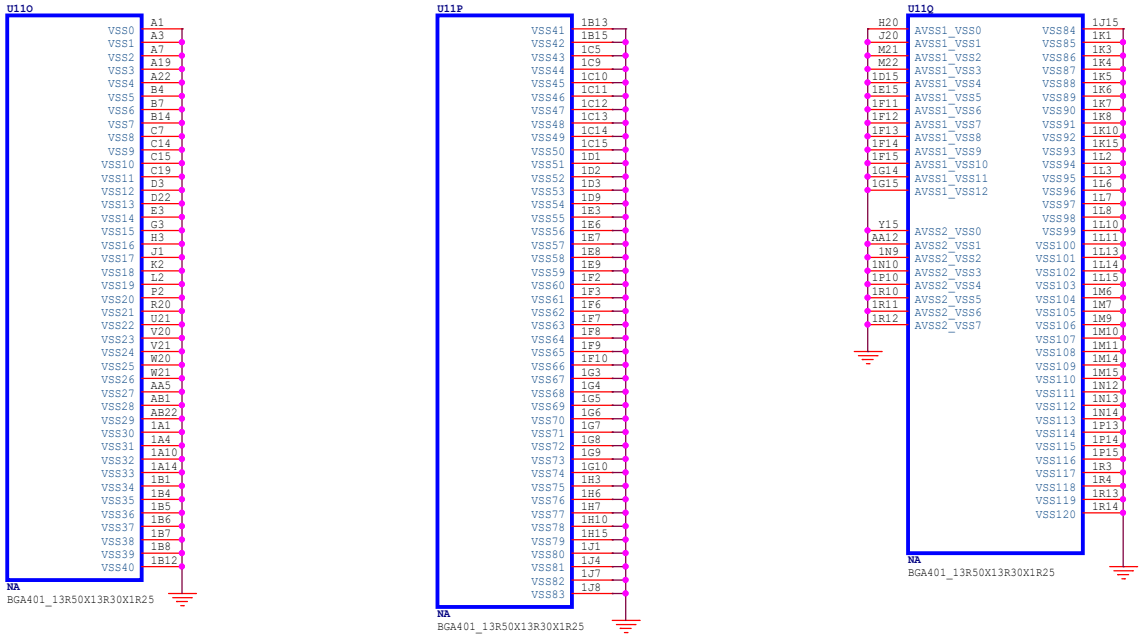
RK3528_N(POWER)



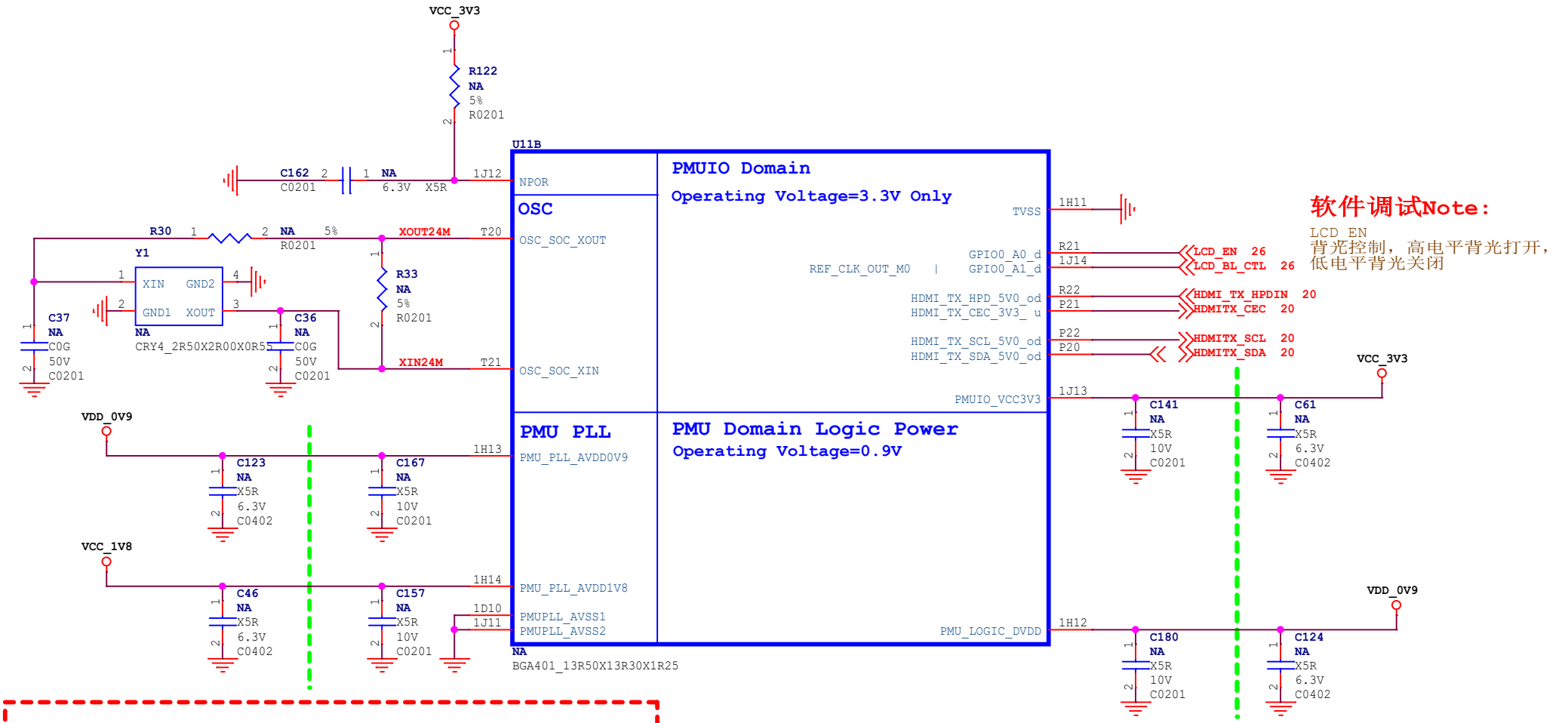
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_O/P/Q(GND)



HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	02.RK3528 Power/GND		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	3 of 27

RK3528_B(OSC/PLL/PMUIO Domain)



软件调试Note：

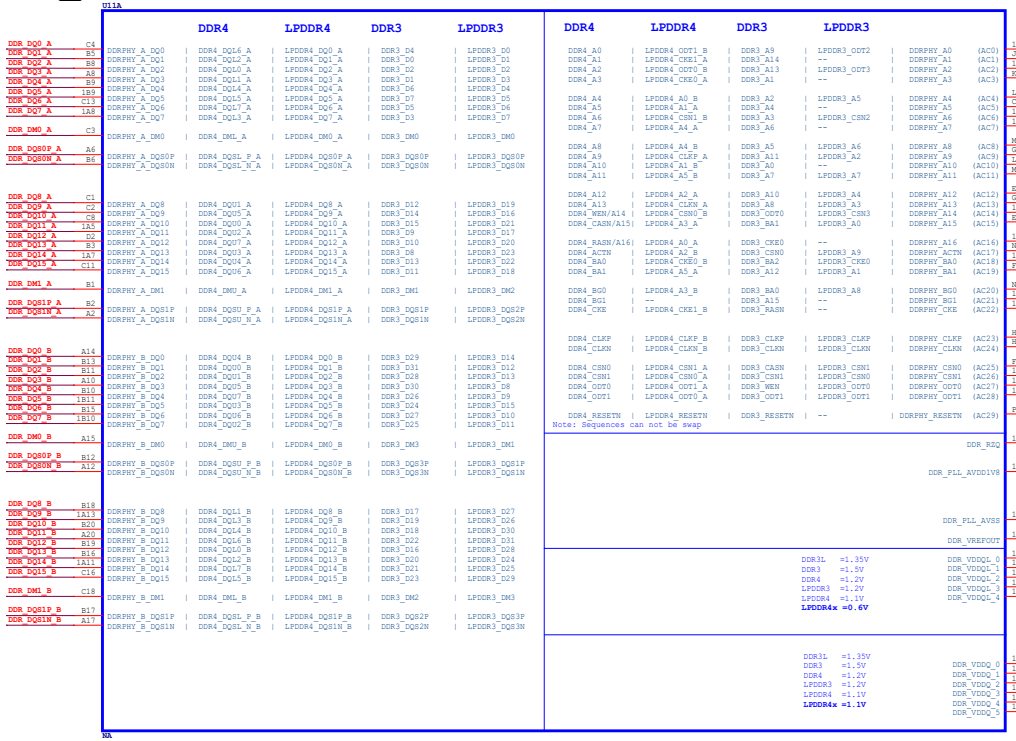
LCD_EN
背光控制，高电平背光打开，
低电平背光关闭

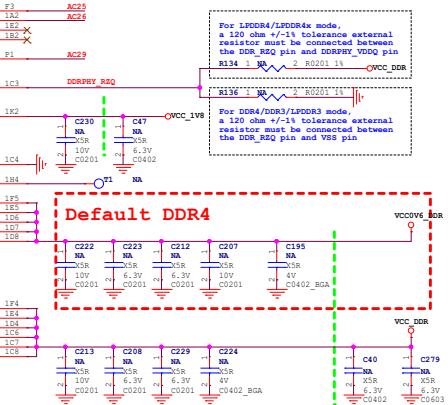
Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	03.RK3528 OSC/PLL/PMUIO		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	4 of 27

RK3528_A(DDR PHY)





Note:
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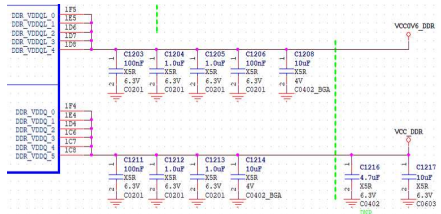
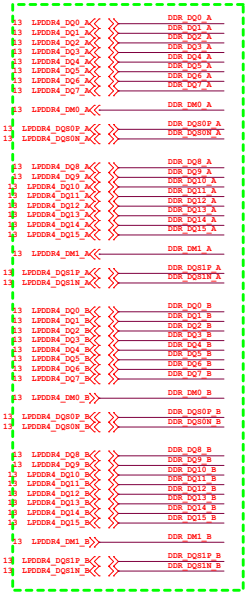
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

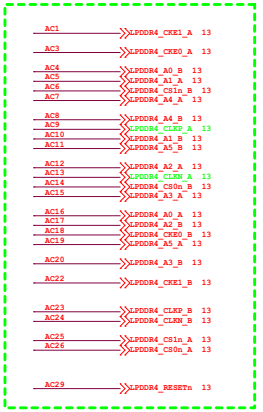
Note:
LPDDR4x mode:
Pin 1F5,1E5,1D6,1D7,1D8 connected to VCC0V6_DDR power supply
For example



LPDDR4/4x DQ



LPDDR4/4x AC



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Project:	RK3528_H29K		
File:	04.RK3528 DDR Controller		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
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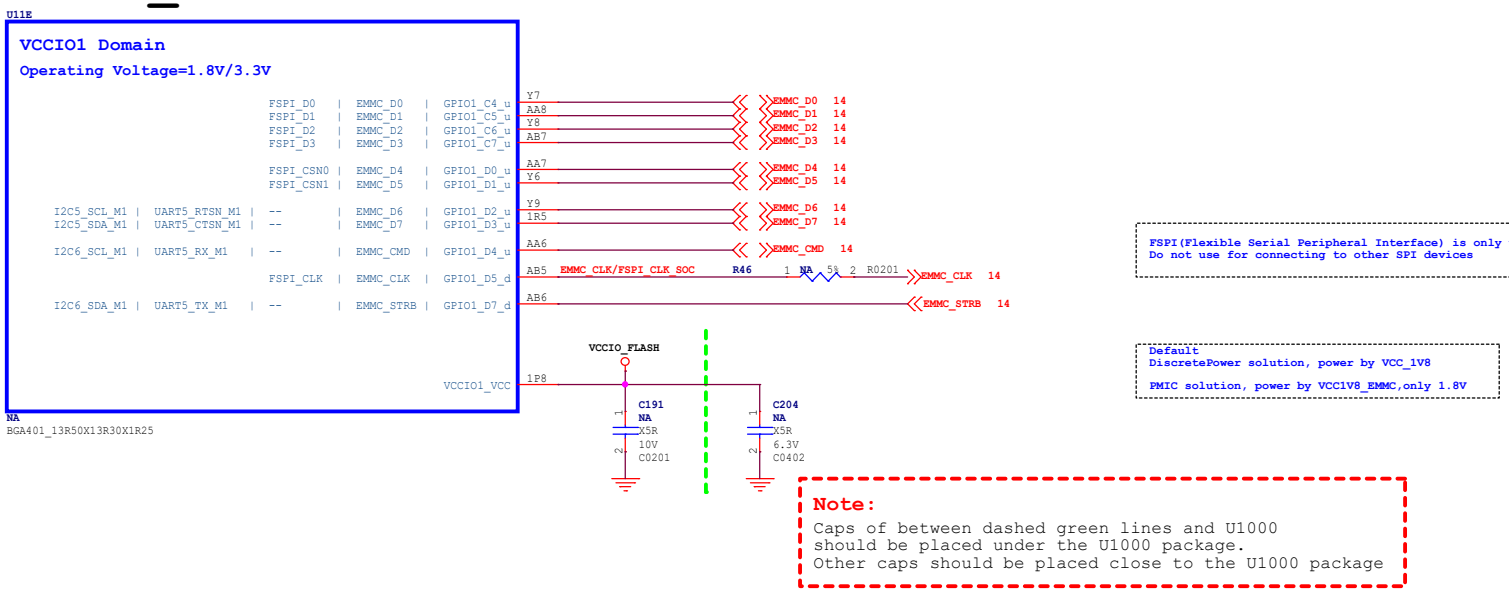
RK3528_E(VCCIO1 Domain)



FSPI(Flexible Serial Peripheral Interface) is only used to connect SPI Flash/Memory devices.
Do not use for connecting to other SPI devices

Default
DiscretePower solution, power by VCC_1V8

PMIC solution, power by VCC1V8_EMMC,only 1.8V

Note:
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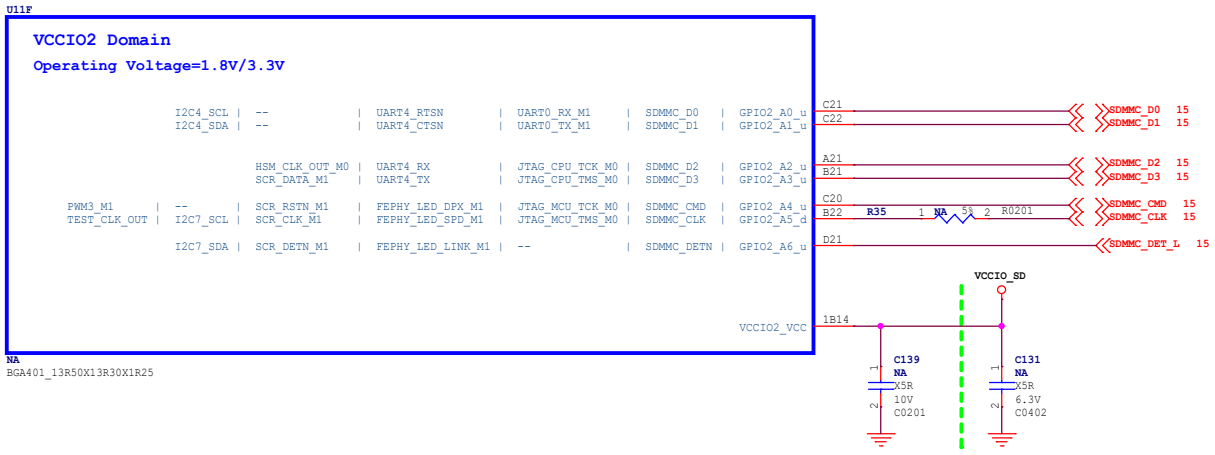
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

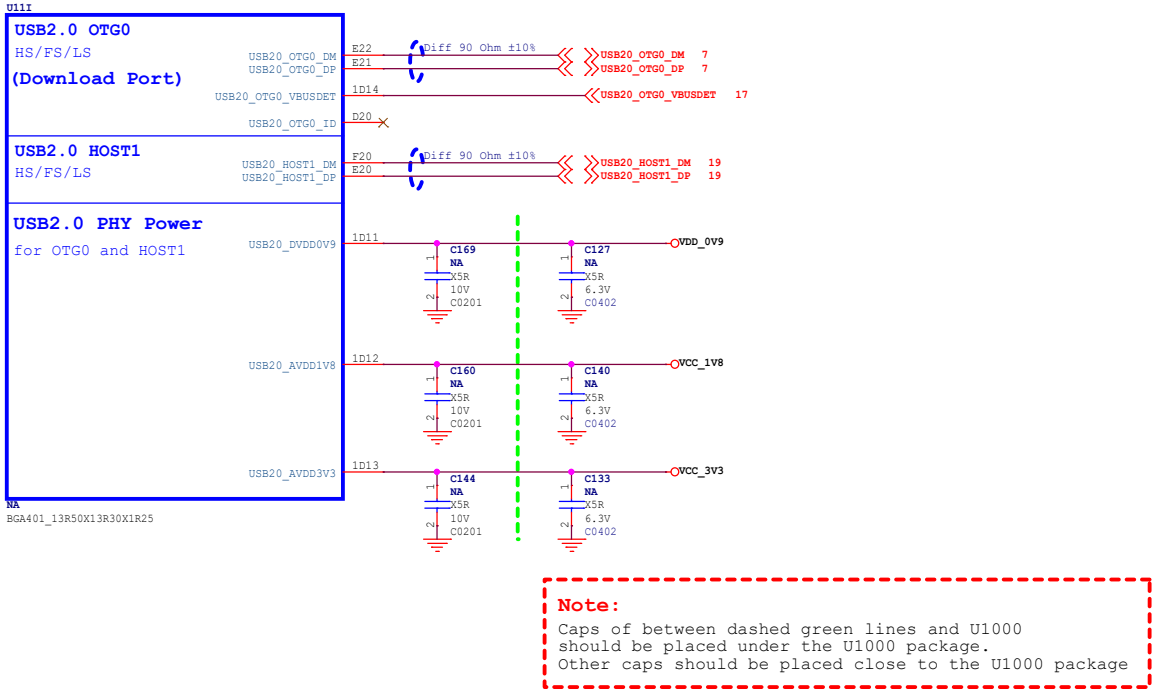
RK3528_F(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

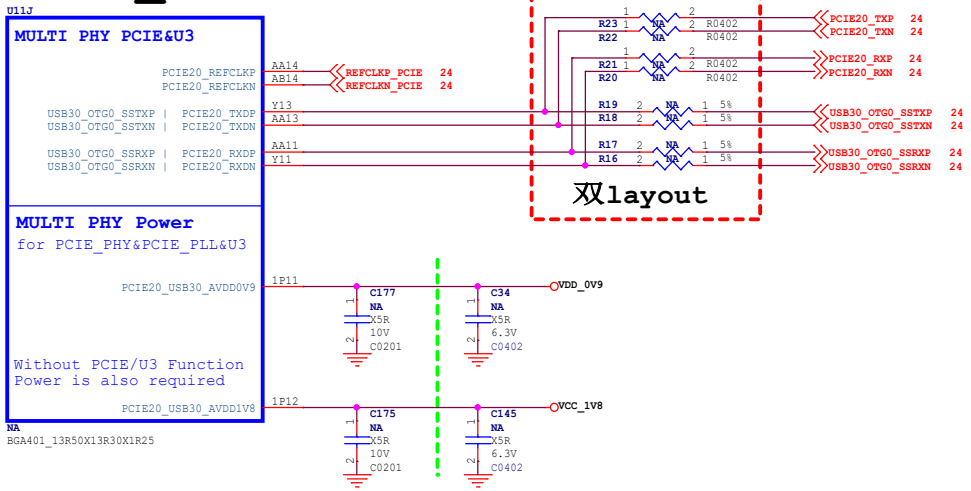
HINLINK		
Project:	RK3528_H29K	
File:	05.RK3528 FLASH/SD Controller	
Date:	Wednesday, March 05, 2025	Rev: <Revision>
Designer:	<designer>	Sheet: 6 of 27

RK3528_I(USB2.0 OTG/HOST)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

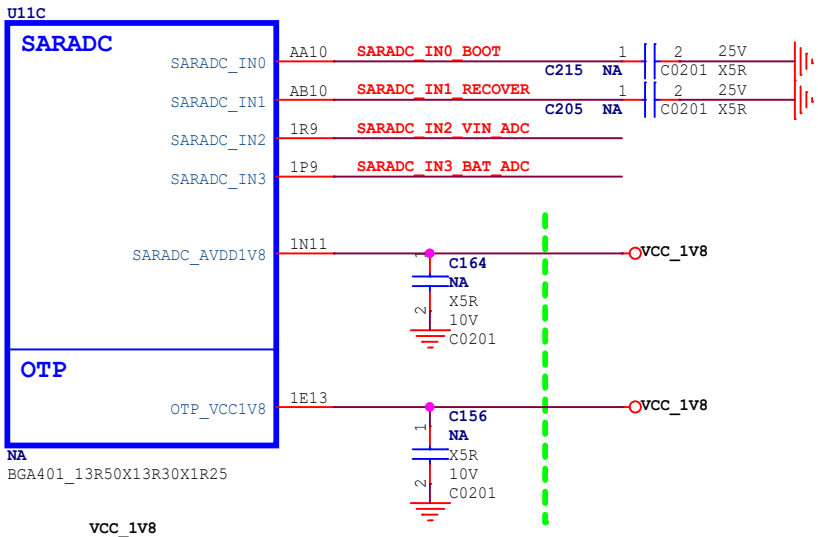
RK3528_J(PCIE2.0/U3 PHY)

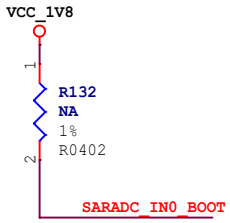


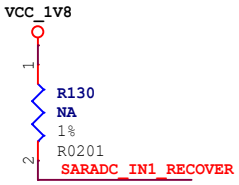
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

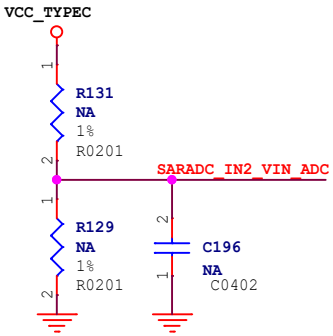
HINLINK			
Project:	RK3528_H29K		
File:	06.RK3528 USB/PCIE Controller		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	7 of 27

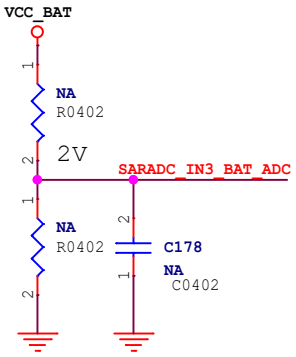
RK3528_C(Saradc/OTP)











输入电压监测
输入电压=读数电压X11
如读数电压1.0V，则输入电压对于1.0X11=11

电池监测
电池电压=读数电压X6.1
如读数电压1.2V，则电池对于1.2X6.1=7.32V

TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB

HINLINK			
Project:	RK3528_H29K		
File:	07.RK3528 SARADC/OTP		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
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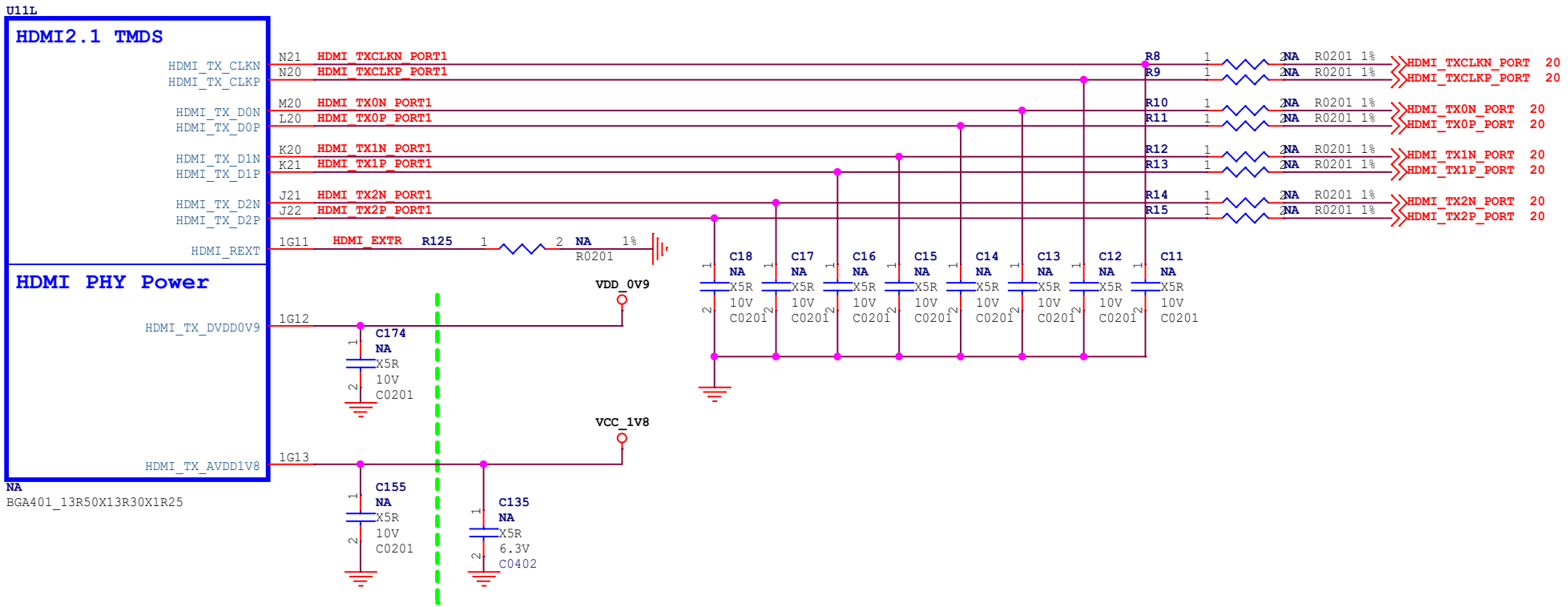
RK3528_L(HDMI PHY)



Note:

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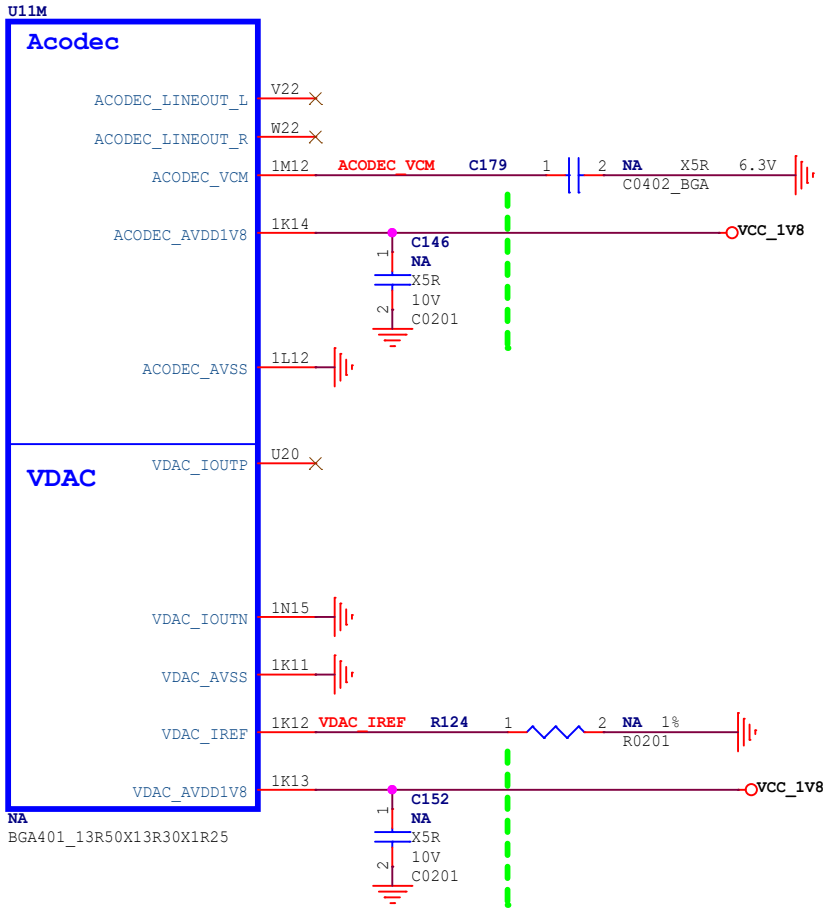
Other caps should be placed close to the U1000 package

HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	08.RK3528 HDMI Interface		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	9 of 27

RK3528_M(Acodec/VDAC)



Note:

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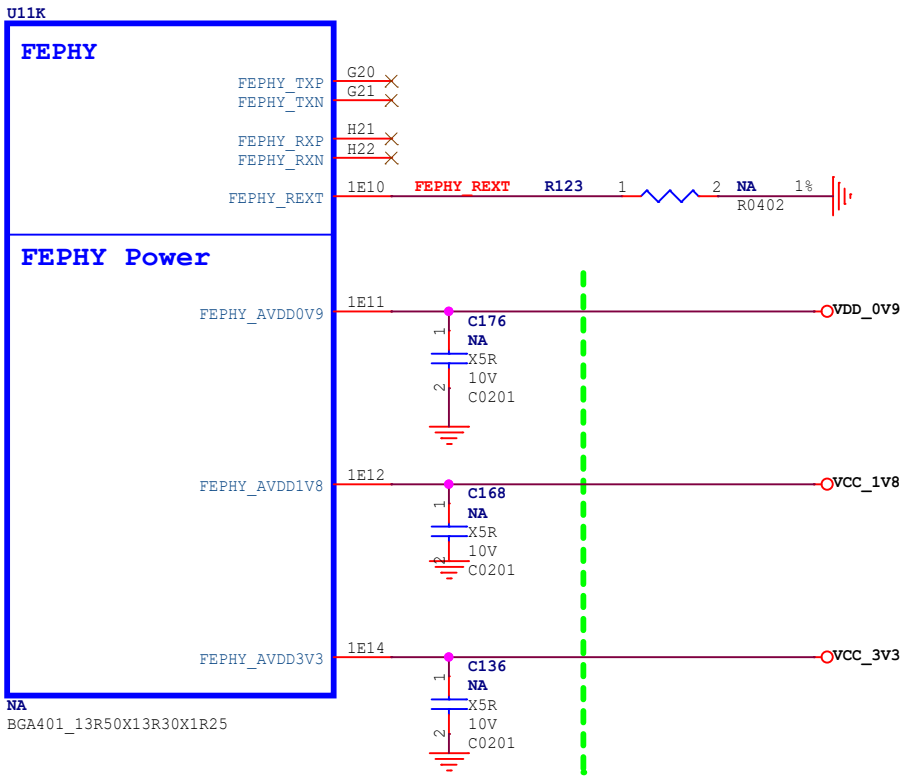
Other caps should be placed close to the U1000 package

HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	09.RK3528 AV OUT		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	10 of 27

RK3528_K(Embed FEPHY)



Note:

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should be placed under the U1000 package.
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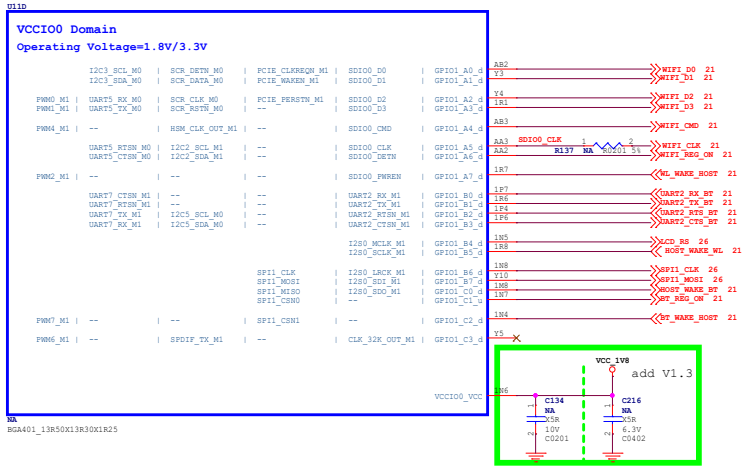
HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	10.RK3528 Embed FEPHY		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	11 of 27

RK3528_D(VCCIO0 Domain)



软件调试Note:
H29K与RT2一模一样，就是新增了：
5G模块和5G相关IO
屏幕IO

软件调试Note:
SPI彩色屏幕

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
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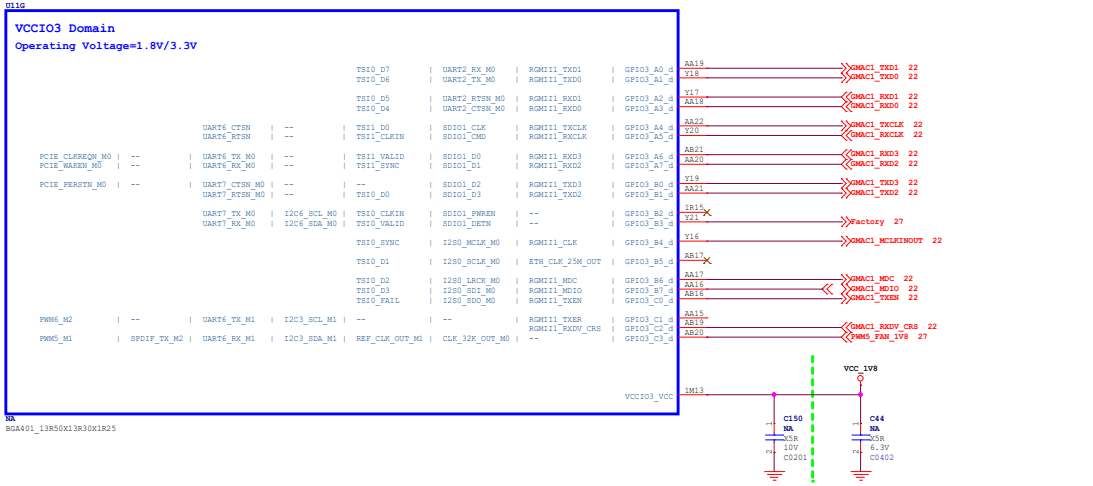
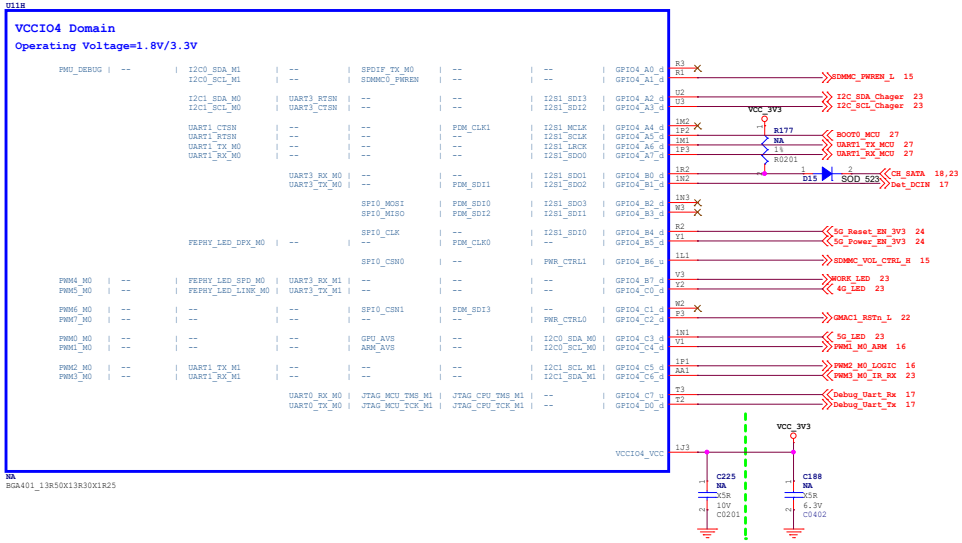
RK3528_G(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_H(VCCIO4 Domain)



软件调试Note:
CH_SATA
电池充满电状态捕获，低电平为充电，高电平为充满或者关闭

Det_DCIN
监测TYPE-C有电源输入

5G_Reset_EN_3V3
输出高店电平，5G模块复位引脚则为低

GPIO4_C0的4G LED
在CPE中代表4G网络，在安卓系统中代表网络连接

GPIO4_C3的5G LED
在CPE中代表5G网络

Note:
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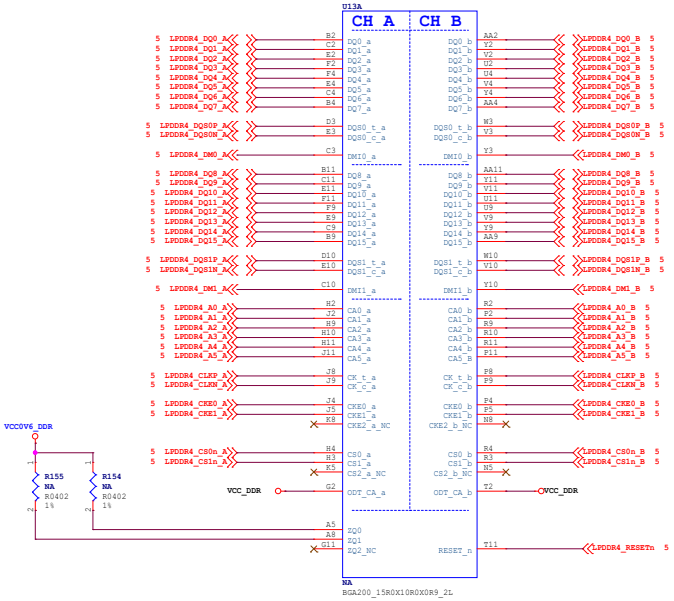
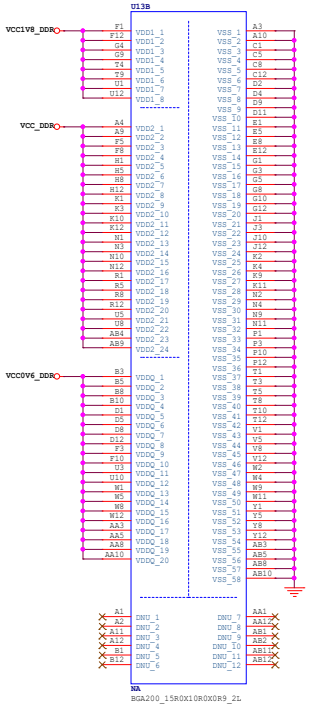
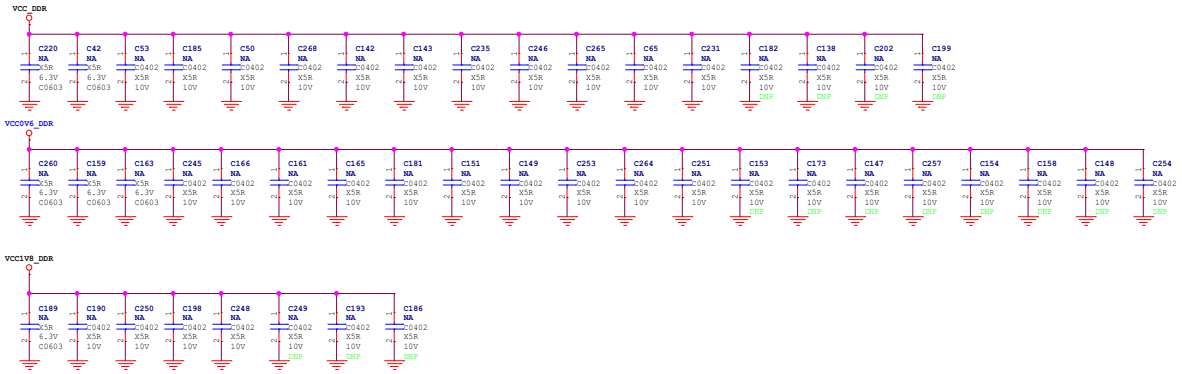
HINLINK		
Project:	RK3528_H29K	HINLINK
File:	11.RK3528_1.8V/3.3V GPIO	
Date:	Wednesday, March 05, 2025	Rev: <Revision>
Designer:	<designer>	Sheet: 12 of 27

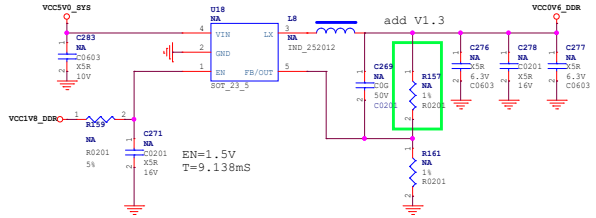
LPDDR4X 200Ball



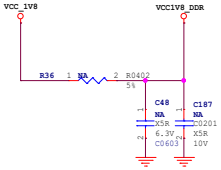




VCC0V6_DDR



VCC1V8_DDR



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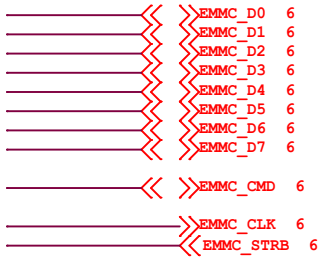
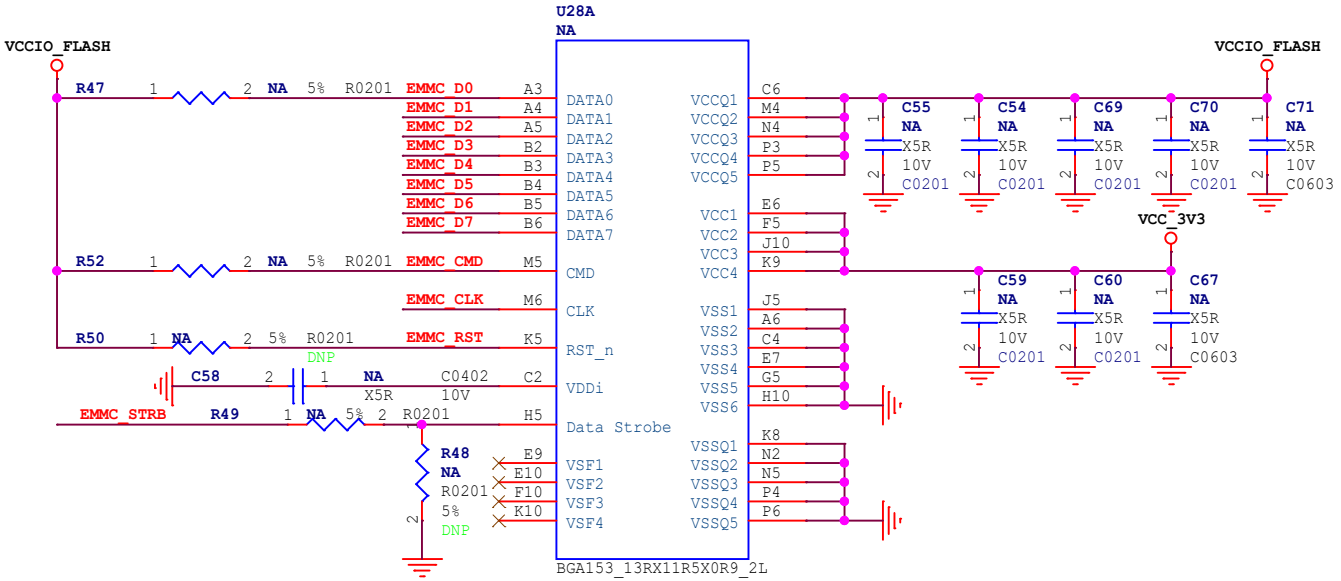
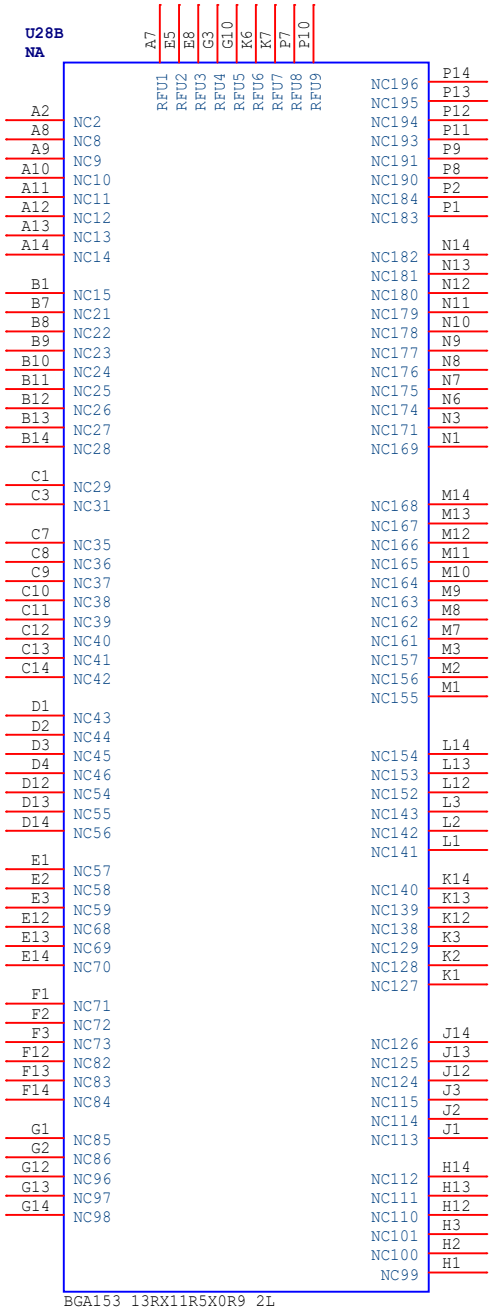
Project:	RK3528_H29K	
File:	12.DRAM-LPDDR4X_1X32bit_200B	
Date:	Wednesday, March 05, 2025	Rev: <Revision>
Designer:	<designer>	Sheet: 13 of 27

EMMC

FSPI

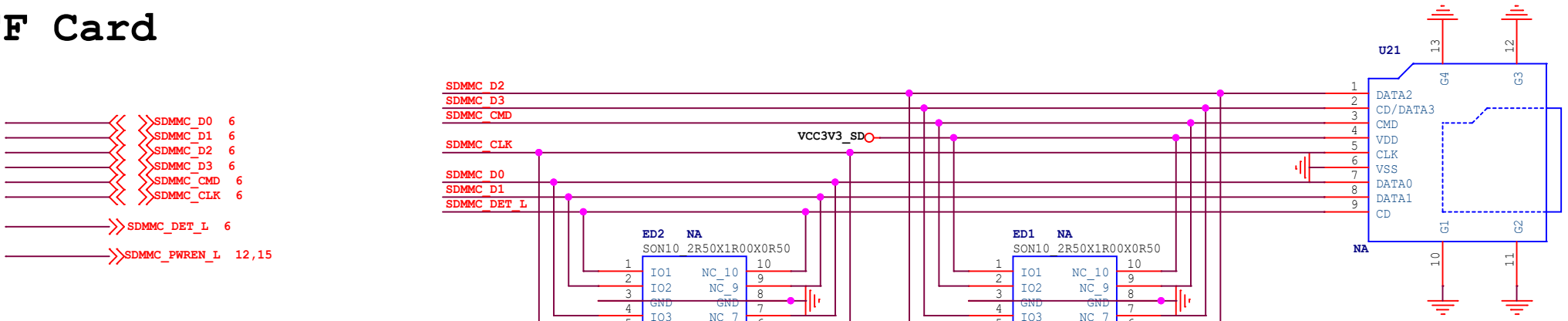




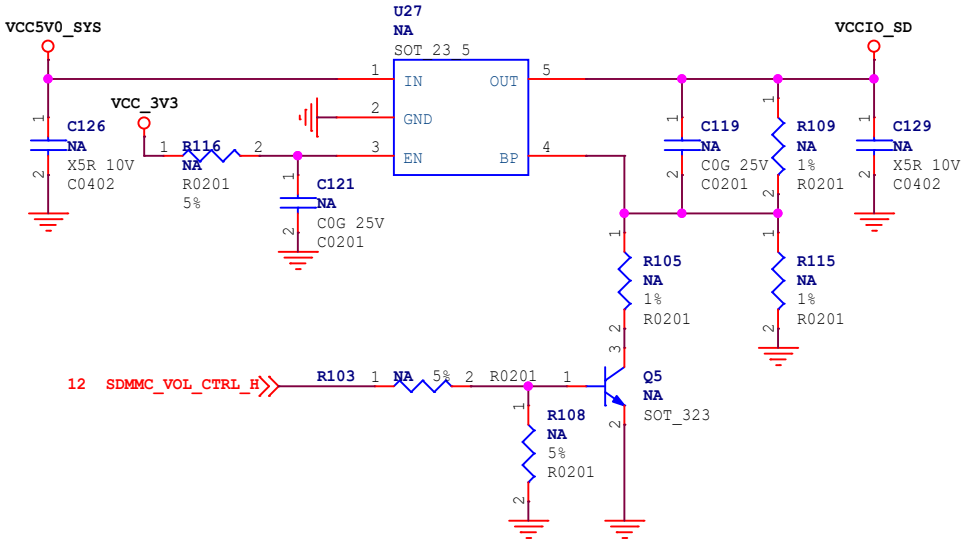


HINLINK			
Project:	RK3528_H29K		
File:	13.Flash-eMMC		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	14 of 27

TF Card

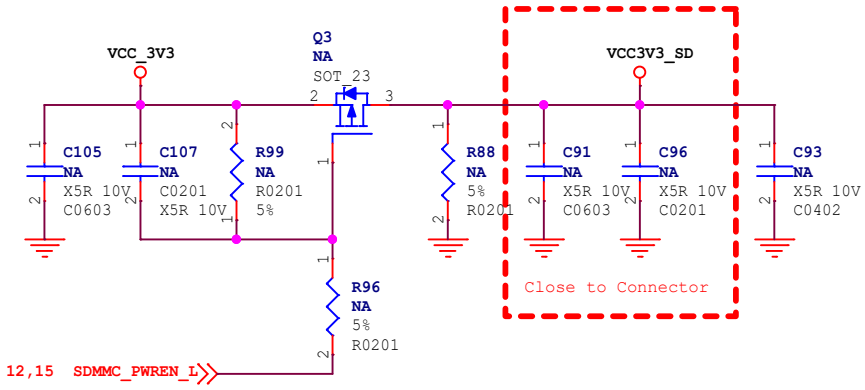


VCCIO_SD



SDIO2.0 SDMMC0_VOL_CTRL=H VCCIO_SD=3.34V(Default)
SDIO3.0 SDMMC0_VOL_CTRL=L VCCIO_SD=1.816V

VCC3V3_SD



SDMMC_PWREN=L VCC_SD=3.3V(Default)
SDMMC_PWREN=H VCC_SD=0V

HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	14.Flash-Micro-SD Card		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
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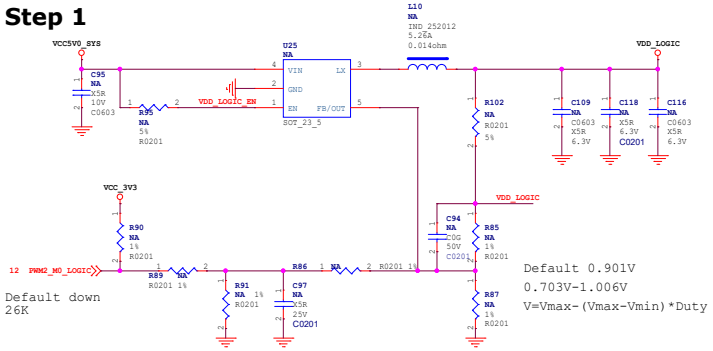
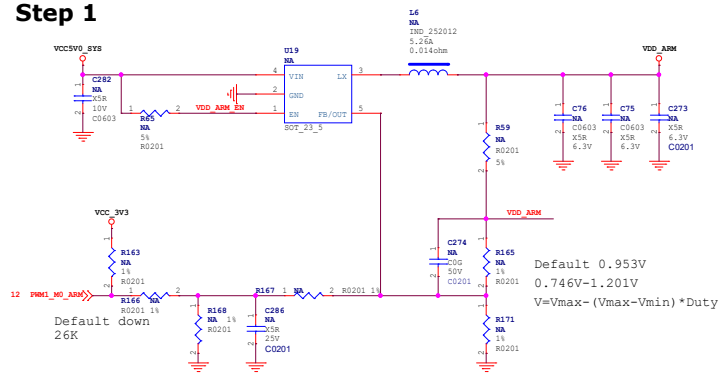
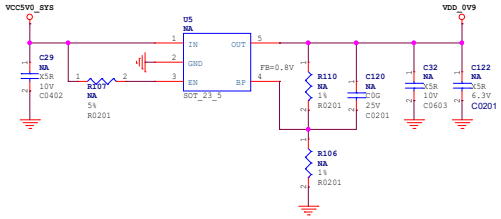
VCC5V0_SYS-->VDD_LOGIC
Step 1



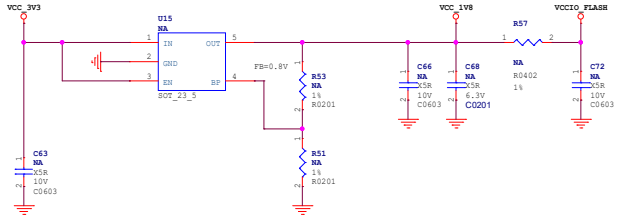
VCC5V0_SYS-->VDD_ARM
Step 1



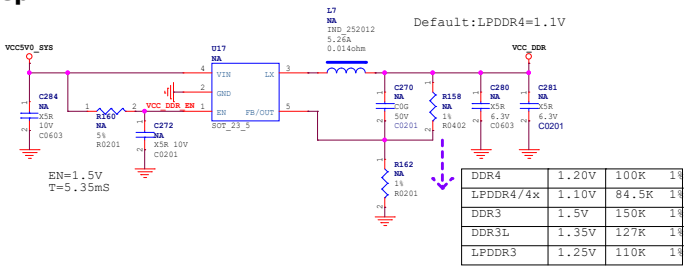
VCC5V0_SYS-->VDD_0V9
Step 1



VCC_3V3->VCC_1V8(LDO)
Step 2

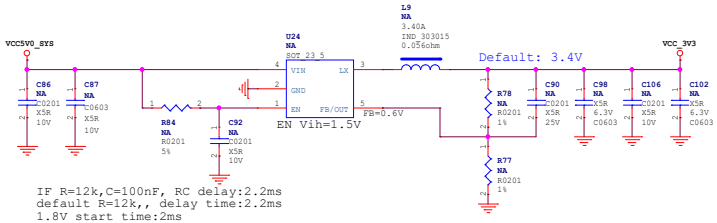


VCC5V0_SYS-->VCC_DDR
Step 2



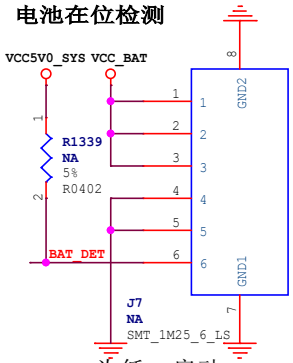
DDR4	1.20V	100K 1%
LPDDR4/4x	1.10V	84.5K 1%
DDR3	1.5V	150K 1%
DDR3L	1.35V	127K 1%
LPDDR3	1.25V	110K 1%

VCC5V0_SYS-->VCC_3V3
Step 2



HINLINK		
Project:	RK3528_H29K	HINLINK
File:	15.Power-DiscretePower	
Date:	Wednesday, March 05, 2025	Rev: <Revision>
Designer:	<designer>	Sheet: 16 of 27

电池在位检测

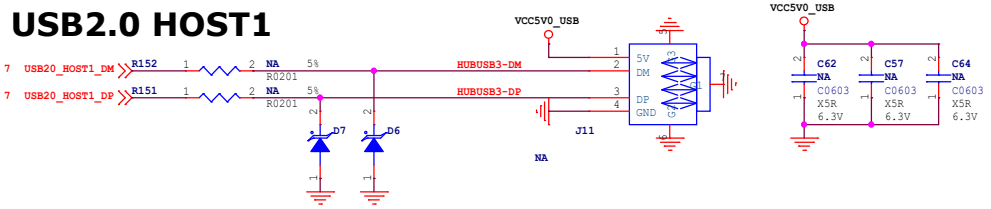


为低，启动U9
为高，关闭U9
电池在位检测

将5 6脚短路即可大电流

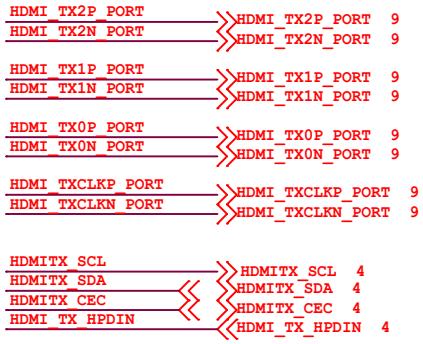
HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	17.Power_Charge		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	18 of 27

USB2.0 HOST1

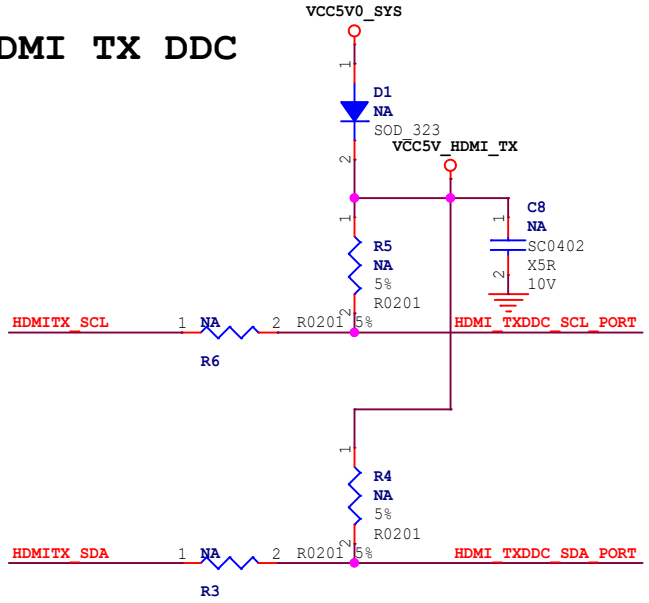


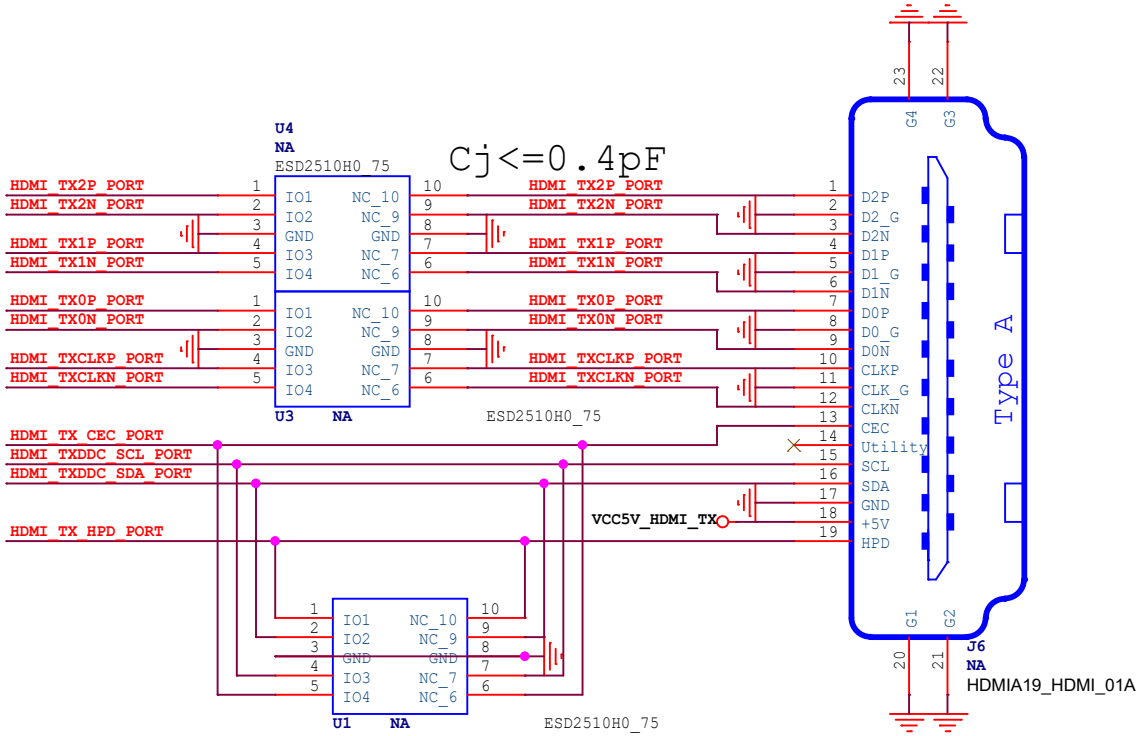
HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	18.USB_A		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	19 of 27

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC
HDMI_TX_HPDIN

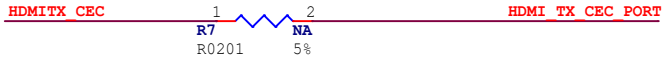


HDMI TX DDC

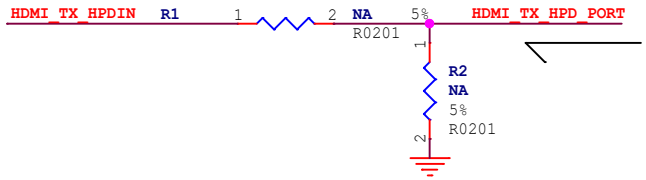




HDMI TX CEC

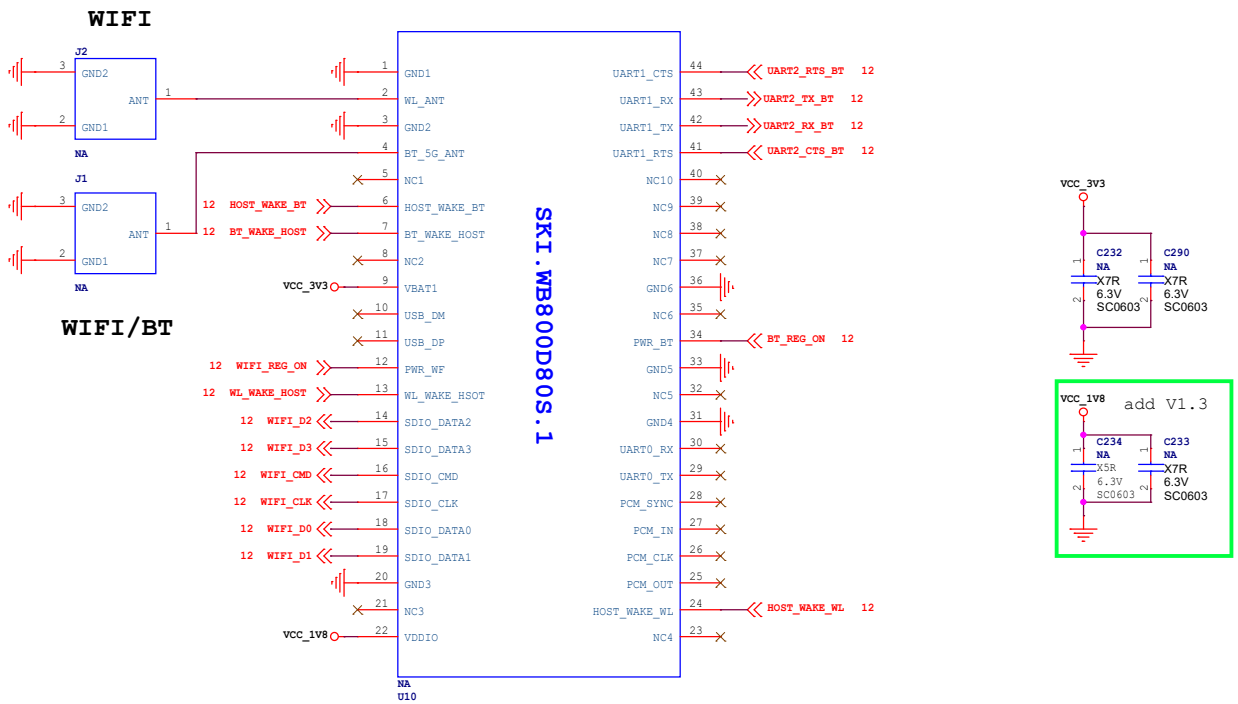


HDMI TX HPD



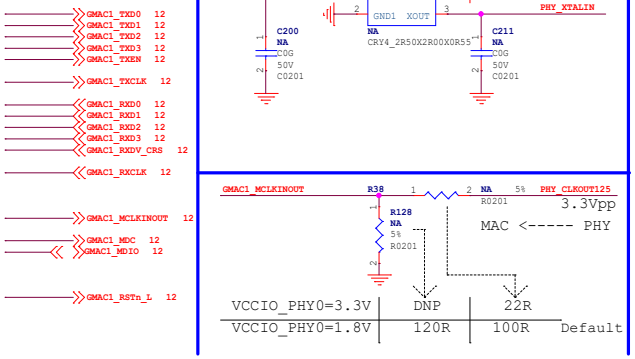
Rockchip Confidential

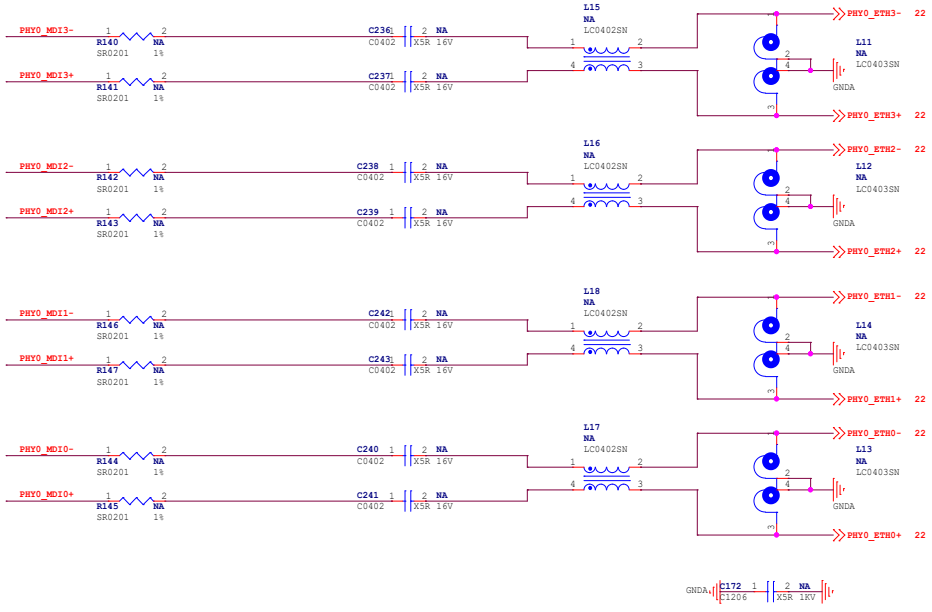
HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	19.VO-HDMI2.0 TX		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	19 of 27

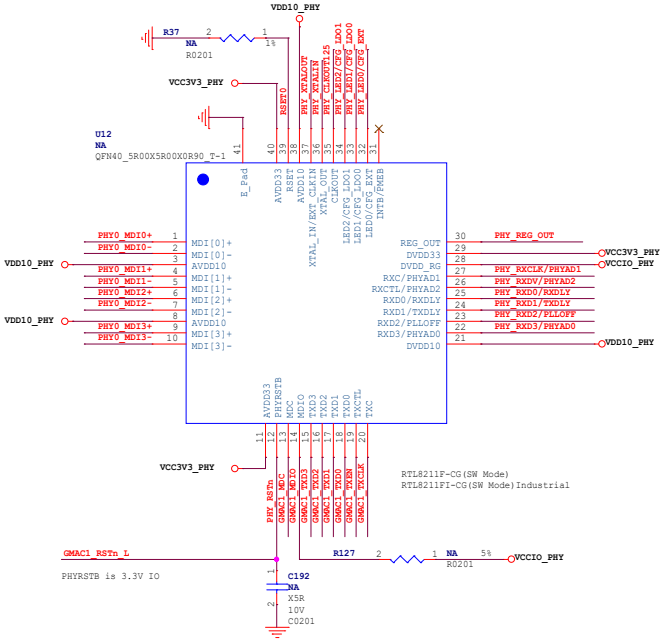


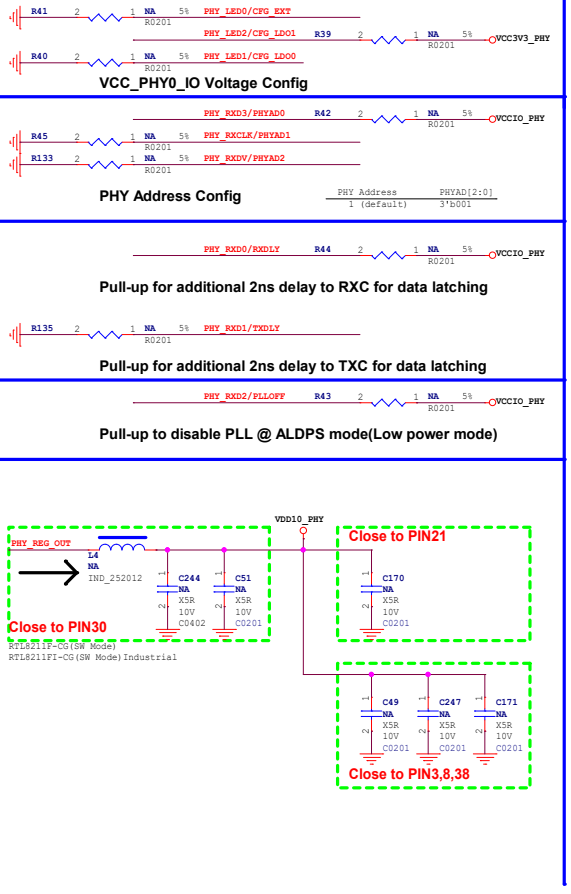
HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	20.SDIO WIFI		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	21 of 27

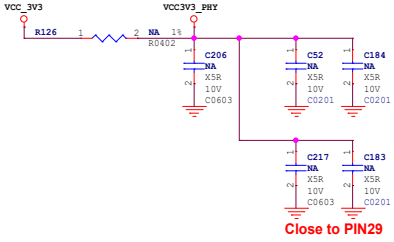
RGMII

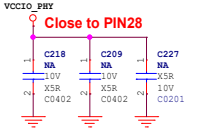






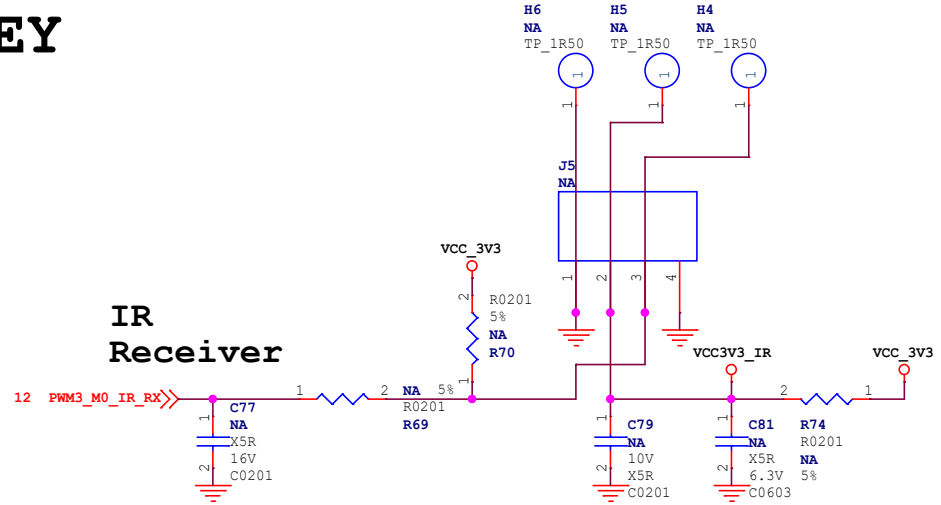






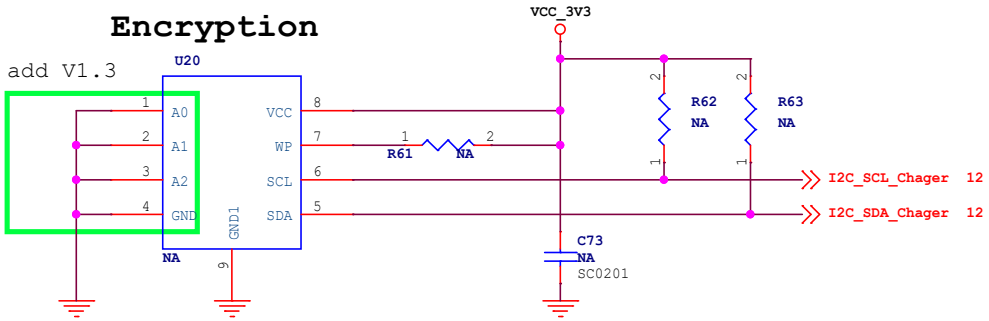
HINLINK			
Project:	RK3528_H29K		
File:	21.Ethernet-GEPHY_RGMII		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	22 of 27

KEY



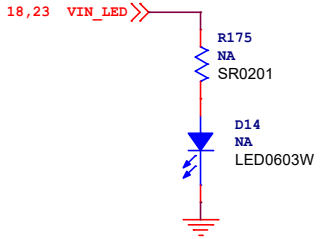
Encryption

add V1.3



7号灯

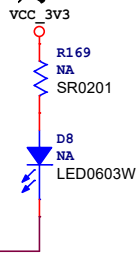
电源灯



红色灯

1号灯

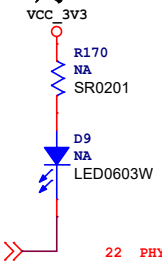
4G灯



红色灯

2号灯

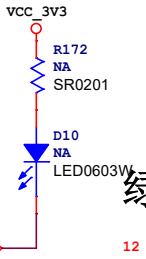
5G灯



蓝灯

3号灯

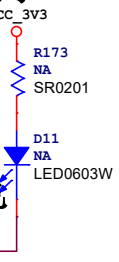
网口



黄灯

4号灯

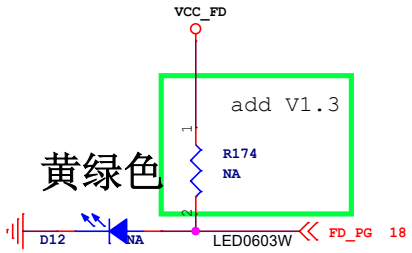
工作灯



绿翠绿色

5号灯

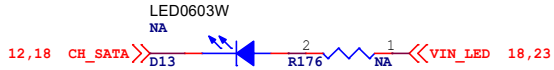
放电灯



黄绿色

6号灯

充电灯



白色灯

HINLINK			
Project:	RK3528_H29K		
File:	22.Key/HW ID/LED		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
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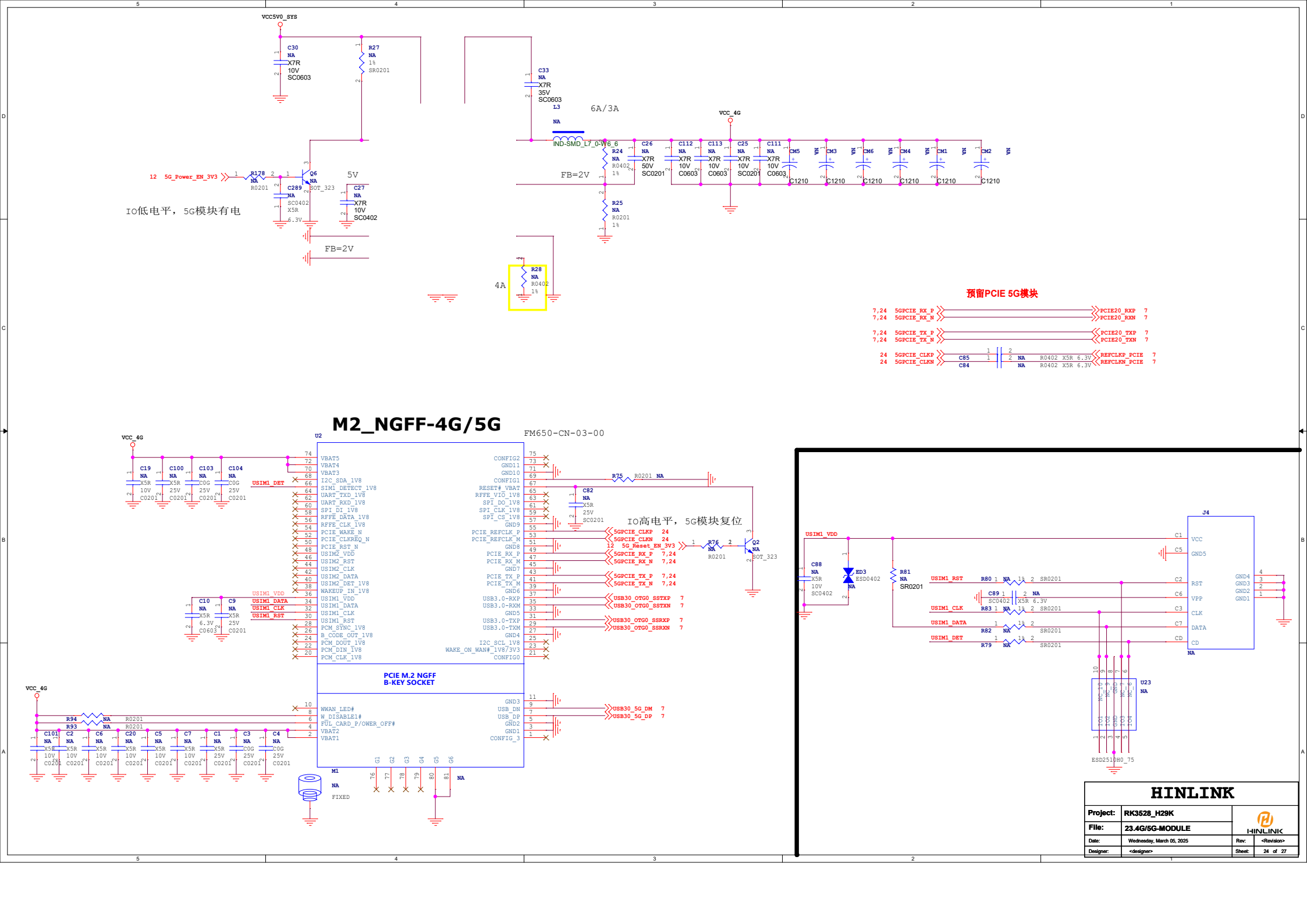
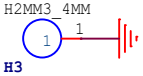
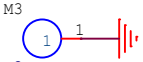

VCC5V0_SYS
C30 NA X7R 10V SC0603
R27 NA 1% SR0201
C33 NA X7R 35V SC0603
L3 NA IND-SMD_L7_0-W6_6
6A/3A
VCC_4G
R24 NA R0402 1%
C26 NA X7R 50V SC0201
C112 NA X7R 10V C0603
C113 NA X7R 10V C0603
C25 NA X7R 10V SC0201
C111 NA X7R 10V C0603
CM5 CM3 CM6 CM4 CM1 CM2 VN
C1210
FB=2V
R25 NA R0201 1%
12 5G_Power_EN_3V3
R178 NA R0201
Q6 NA SOT_323
C289 NA SC0402 X5R 6.3V
C27 NA X7R 10V SC0402
5V
IO低电平，5G模块有电
FB=2V
R28 NA R0402 1%
4A
预留PCIE 5G模块
7,24 5GPCIE_RX_P
7,24 5GPCIE_RX_N
PCIE20_RXP 7
PCIE20_RXN 7
7,24 5GPCIE_TX_P
7,24 5GPCIE_TX_N
PCIE20_TXP 7
PCIE20_TXN 7
24 5GPCIE_CLKP
24 5GPCIE_CLKN
C85 NA
C84 NA
R0402 X5R 6.3V
REFCLKP_PCIE 7
REFCLKN_PCIE 7
M2_NGFF-4G/5G
FM650-CN-03-00
U2
VCC_4G
C19 C100 C103 C104 NA X5R 10V C0201
C0G 25V C0201
USIM1_DET
VBAT5 VBAT4 VBAT3
I2C_SDA_1V8
SIM1_DETECT_1V8
UART_TXD_1V8
UART_RXD_1V8
SPI_DI_1V8
RFFE_DATA_1V8
RFFE_CLK_1V8
PCIE_WAKE_N
PCIE_CLKREQ_N
PCIE_RST_N
USIM2_VDD
USIM2_RST
USIM2_CLK
USIM2_DATA
USIM2_DET_1V8
WAKEUP_IN_1V8
USIM1_VDD
USIM1_DATA
USIM1_CLK
USIM1_RST
PCM_SYNC_1V8
B_CODE_OUT_1V8
PCM_DOUT_1V8
PCM_DIN_1V8
PCM_CLK_1V8
C10 NA X5R 6.3V C0603
C9 NA X5R 25V C0201
CONFIG2 GND11 GND10 CONFIG1
RESET#_VBAT
RFFE_VIO_1V8
SPI_DO_1V8
SPI_CLK_1V8
SPI_CS_1V8
GND9 GND8 GND7 GND6 GND5 GND4
PCIE_REFCLK_P
PCIE_REFCLK_M
PCIE_RX_P
PCIE_RX_M
PCIE_TX_P
PCIE_TX_M
USB3.0-RXP
USB3.0-RXM
USB3.0-TXP
USB3.0-TXM
I2C_SCL_1V8
WAKE_ON_WAN#_1V8
CONFIG0
R75 R0201 NA
C82 NA X5R 25V SC0201
IO高电平，5G模块复位
5GPCIE_CLKP 24
5GPCIE_CLKN 24
12 5G_Reset_EN_3V3
5GPCIE_RX_P 7,24
5GPCIE_RX_N 7,24
5GPCIE_TX_P 7,24
5GPCIE_TX_N 7,24
USB30_OTG0_SSTXP 7
USB30_OTG0_SSTXN 7
USB30_OTG0_SSRXP 7
USB30_OTG0_SSRXN 7
R76 NA R0201
Q2 NA SOT_323
PCIE M.2 NGFF
B-KEY SOCKET
WWAN_LED#
W_DISABLE1#
FUL_CARD_P/OWER_OFF#
VBAT2
VBAT1
GND3 USB_DN USB_DP GND2 GND1 CONFIG_3
USB30_5G_DM 7
USB30_5G_DP 7
G1 G2 G3 G4 G5 G6
M1 NA FIXED
R94 NA R0201
R93 NA R0201
C101 C2 C6 C20 C5 C7 C1 C3 C4 NA X5R 10V C0201
C0G 25V C0201
USIM1_VDD
C88 NA X5R 10V SC0402
D3 ESD0402 NA
R81 NA SR0201
USIM1_RST R80 NA SR0201
C89 NA SC0402 X5R 6.3V
USIM1_CLK R83 NA SR0201
USIM1_DATA R82 NA SR0201
USIM1_DET R79 NA SR0201
J4
VCC GND5 RST VPP CLK DATA CD
GND4 GND3 GND2 GND1
U23 NA
ESD2510H0_75
HINLINK
Project: RK3528_H29K
File: 23.4G/5G-MODULE
Date: Wednesday, March 05, 2025
Rev: <Revision>
Designer: <designer>
Sheet: 24 of 27

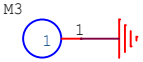
H1
NA
H2MM3_4MM



H3
NA
M3



H2
NA
M3



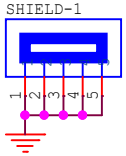
MARK1
NA

MARK3
NA

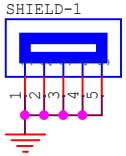
MARK4
NA

MARK2
NA

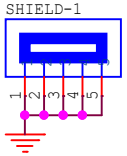
SHIELD2
NA
SHIELD-1



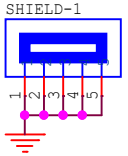
SHIELD8
NA
SHIELD-1



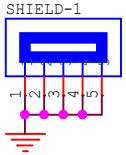
SHIELD1
NA
SHIELD-1



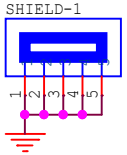
SHIELD6
NA
SHIELD-1



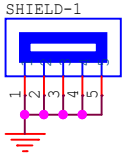
SHIELD5
NA
SHIELD-1



SHIELD3
NA
SHIELD-1

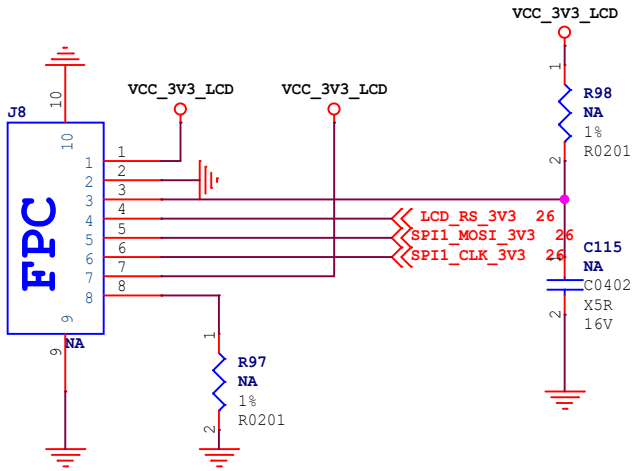


SHIELD7
NA
SHIELD-1

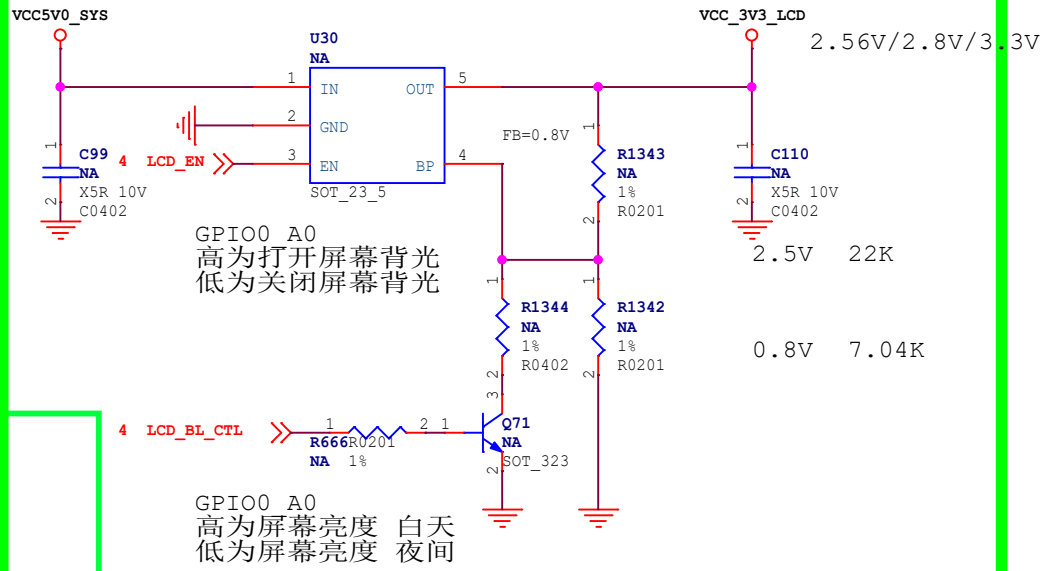


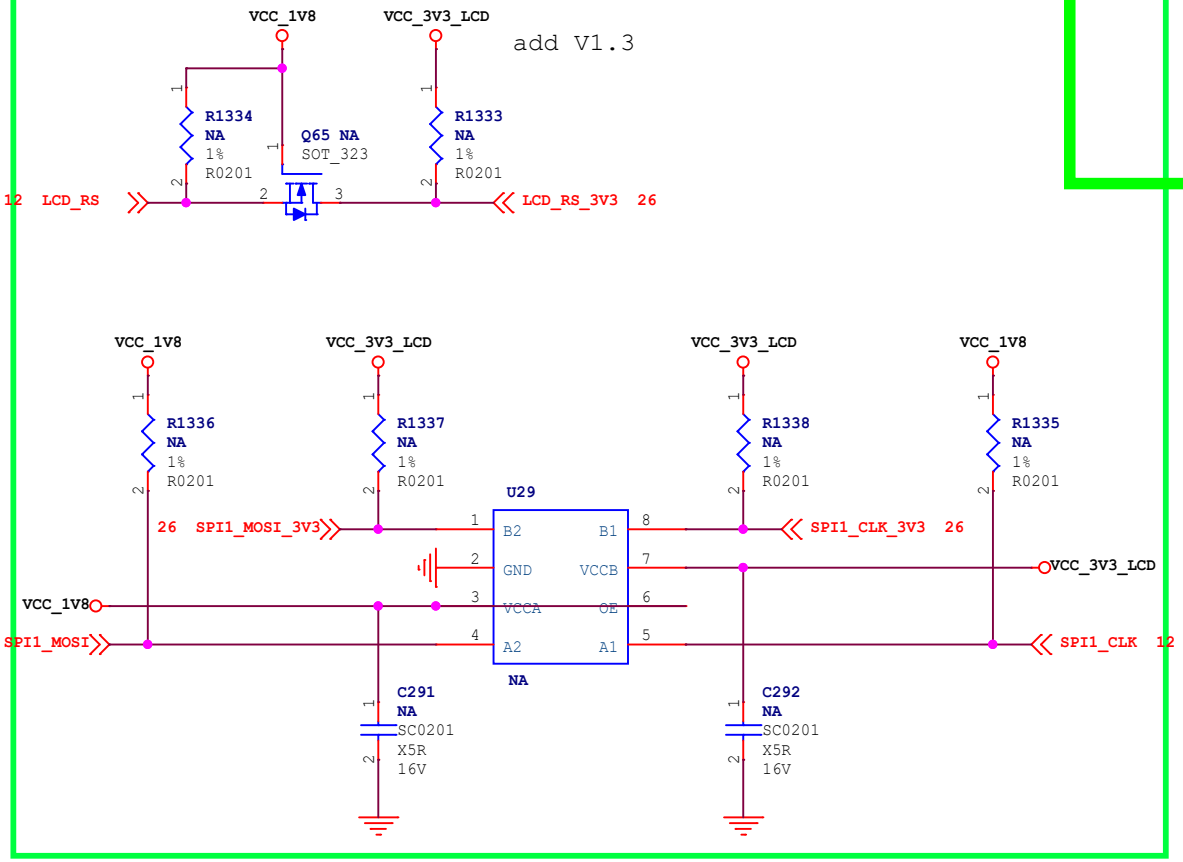
HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	24.Mark/Hole		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	25 of 27

屏幕



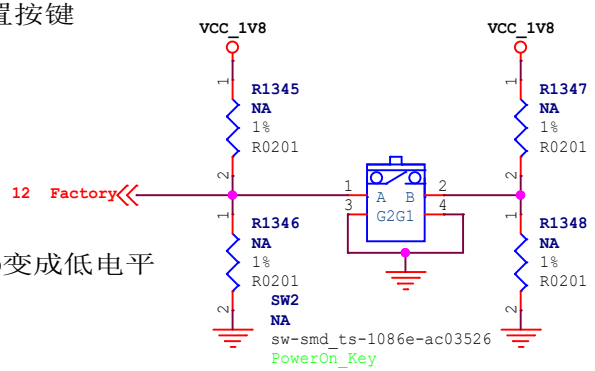
增加背光控制





HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	25.LCD		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	26 of 27

恢复出厂设置按键



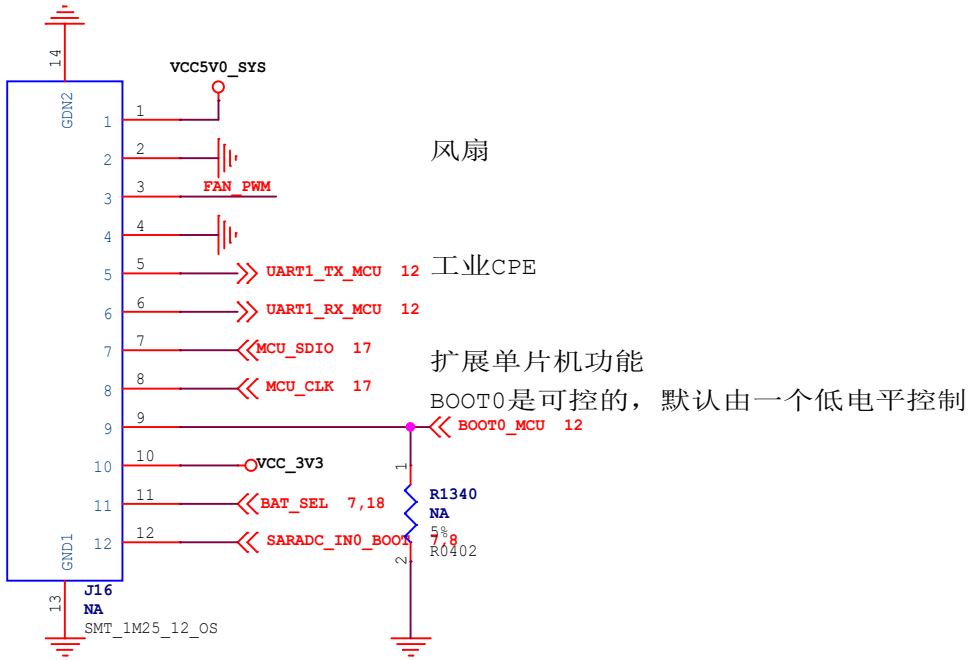
按下去，IO变成低电平

add V1.3

风扇电平转换

add V1.3

add V1.3



风扇

工业CPE

扩展单片机功能

BOOT0是可控的，默认由一个低电平控制

HINLINK			
Project:	RK3528_H29K	HINLINK	
File:	26.MCU+FAN+Factory		
Date:	Wednesday, March 05, 2025	Rev:	<Revision>
Designer:	<designer>	Sheet:	27 of 27